Programmable Logic Replacement Module

Technical Description

1. Purpose

The EKT9320GS84 module is intended as a form-fit functional replacement for the discontinued EPM9320LI84-15 programmable logic device used in pulse-generation circuitry controlling the windings of a phase-shifter group.

Device Parameters

Parameter	Value
Operating voltage	5.0 V ±10%
Operating temperature range	-40 to +85 °C (industrial)
Number of leads	84
Module length	30.226 ±0.127 mm
Module width	30.226 ±0.127 mm
Module height	≤3.00 mm

The module outline dimensions conform to a standard 84-pin Plastic J-Lead Chip Carrier (PLCC84) package in accordance with ASME Y14.5M-1994.

The pinout and functional assignment correspond to the original EPM9320LI84 device. Device operation and pin functions are maintained to preserve compatibility with the original implementation.

2. Design

The EKT9320GS84 module is implemented using a modern programmable logic device manufactured by a Chinese company. Because the core logic operates with external signal levels not exceeding 3.3 V, level-shifting buffer devices are used to provide compatibility with 5 V external interfaces.

A single-gate logic device provides the tri-state output function. A low-dropout linear regulator generates the internal 3.3 V supply rail.

All electronic components used in the module are rated for the industrial temperature range of -40 to +85°C.

The circuit schematic is included in the source technical documentation.

3. Pin Assignments

Pin 1 location and pin numbering follow the PLCC84 package convention used by the original EPM9320LI84 device.

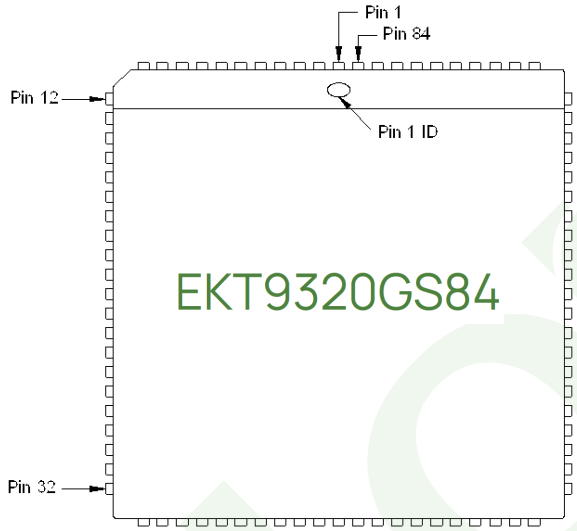


Table 1. Device Pin Assignments

Pin	Direction	Type	Signal	Description
1	Input	Hi-Z Input	STR_ADR	Pulse-width value write-strobe input to register
2	Output	Push-Pull Output	OUT_PR8	Pulse-width generator output, channel 8
3	Output	Push-Pull Output	OUT_PR7	Pulse-width generator output, channel 7
4	Output	Push-Pull Output	OUT_PR6	Pulse-width generator output, channel 6
5	Output	Push-Pull Output	OUT_PR5	Pulse-width generator output, channel 5
6	-	Power	GND	Ground
7	Output	Push-Pull Output	OUT_PR4	Pulse-width generator output, channel 4

Table 1. Device Pin Assignments (continued)

Pin	Direction	Type	Signal	Description
8	Output	Push-Pull Output	OUT_PR3	Pulse-width generator output, channel 3
9	Input	Hi-Z Input	SEL	Address-space select input
10	Output	Push-Pull Output	OUT_PR2	Pulse-width generator output, channel 2
11	Output	Push-Pull Output	OUT_PR1	Pulse-width generator output, channel 1
12	Output	Push-Pull Output	OUT_PR0	Pulse-width generator output, channel 0
13	Input	Hi-Z Input	RST	Global reset input
14	-	Power	VCC5V	5.0 V supply input
15	-	Power	VCC5V	5.0 V supply input
16	-	NC	-	Not connected
17	-	NC	-	Not connected
18	-	Power	GND	Ground
19	-	NC	-	Not connected
20	-	NC	-	Not connected
21	-	Power	VCC5V	5.0 V supply input
22	-	NC	-	Not connected
23	-	NC	-	Not connected
24	-	Power	GND	Ground
25	-	Power	GND	Ground
26	-	NC	-	Not connected
27	-	NC	-	Not connected
28	-	Power	GND	Ground
29	-	NC	-	Not connected
30	Output	Push-Pull Output	TDO	JTAG data output
31	Input	Hi-Z Input	INT	Pulse-width generator flip-flop reset input
32	Input	Hi-Z Input	STR_SUMM	Pulse-width generator enable input
33	Input	Hi-Z Input	ADR_IN3	Monitor channel select input, bit 3
34	Input	Hi-Z Input	SEL	Decoder enable input
35	-	NC	-	Not connected
36	Output	3-State Output	IK1	Pulse-width channel multiplexer monitor output
37	-	Power	VCC5V	5.0 V supply input
38	Input	Hi-Z Input	ADR_IN0	Monitor channel select input, bit 0
39	Input	Hi-Z Input	ADR_IN1	Monitor channel select input, bit 1
40	-	NC	-	Not connected

Table 1. Device Pin Assignments (continued)

Pin	Direction	Type	Signal	Description
41	Input	Hi-Z Input	ADR_IN2	Monitor channel select input, bit 2
42	Input	Hi-Z Input	TDI	JTAG data input
43	Input	Hi-Z Input	TCK	JTAG clock input
44	Input	Hi-Z Input	ADR_IN4	Monitor channel select input, bit 4
45	Input	Hi-Z Input	ADR_IN5	Monitor channel select input, bit 5
46	-	NC	-	Not connected
47	Input	Hi-Z Input	DATA_IN5	Pulse-width setting input, bit 5
48	-	Power	GND	Ground
49	Input	Hi-Z Input	DATA_IN0	Pulse-width setting input, bit 0
50	Input	Hi-Z Input	DATA_IN4	Pulse-width setting input, bit 4
51	-	NC	-	Not connected
52	-	NC	-	Not connected
53	Input	Hi-Z Input	DATA_IN3	Pulse-width setting input, bit 3
54	Input	Hi-Z Input	DATA_IN2	Pulse-width setting input, bit 2
55	Input	Hi-Z Input	TMS	JTAG state-machine control input
56	-	Power	VCC5V	5.0 V supply input
57	-	Power	VCC5V	5.0 V supply input
58	-	NC	-	Not connected
59	-	NC	-	Not connected
60	-	Power	VCC5V	5.0 V supply input
61	-	Power	GND	Ground
62	-	NC	-	Not connected
63	-	NC	-	Not connected
64	-	Power	VCC5V	5.0 V supply input
65	-	NC	-	Not connected
66	-	NC	-	Not connected
67	-	Power	GND	Ground
68	-	NC	-	Not connected
69	-	NC	-	Not connected
70	-	Power	GND	Ground
71	-	Power	VCC5V	5.0 V supply input
72	Input	Hi-Z Input	STR_C	Multiplexer enable input
73	Input	Hi-Z Input	DATA_IN1	Pulse-width setting input, bit 1
74	Output	Push-Pull Output	OUT_PR17	Pulse-width generator output, channel 17

Table 1. Device Pin Assignments (continued)

Pin	Direction	Type	Signal	Description
75	Output	Push-Pull Output	OUT_PR16	Pulse-width generator output, channel 16
76	Output	Push-Pull Output	OUT_PR15	Pulse-width generator output, channel 15
77	Output	Push-Pull Output	OUT_PR14	Pulse-width generator output, channel 14
78	Output	Push-Pull Output	OUT_PR13	Pulse-width generator output, channel 13
79	-	Power	VCC5V	5.0 V supply input
80	Output	Push-Pull Output	OUT_PR12	Pulse-width generator output, channel 12
82	Output	Push-Pull Output	OUT_PR11	Pulse-width generator output, channel 11
82	Output	Push-Pull Output	OUT_PR10	Pulse-width generator output, channel 10
83	Output	Push-Pull Output	OUT_PR19	Pulse-width generator output, channel 9
84	Input	Hi-Z Input	F_ET	Pulse-width generator clock input

Pin Groups

Not Connected (NC): 16, 17, 19, 20, 22, 23, 26, 27, 29, 35, 40, 46, 51, 52, 58, 59, 62, 63, 65, 66, 68, 69.

Ground (GND): 6, 18, 24, 25, 48, 61, 67, 70.

5 V Supply (VCC5V): 14, 15, 21, 28, 37, 56, 57, 60, 64, 71, 79.

Table 2. JTAG Programming Pins

Pin	JTAG Signal	Direction
43	TCK	Input
42	TDI	Input
55	TMS	Input
30	TDO	Output

The external connection requirements for the programming pins of the EKT9320GS84 module are identical to those of the Altera EPM9320LI84 programmable logic device.

Recommended JTAG Connections

- TCK: external 1 kΩ pull-down resistor to ground.
- TDI: external 10 kΩ pull-up resistor to +5.0 V.
- TMS: external 10 kΩ pull-up resistor to +5.0 V.
- TDO: optional external 10 kΩ pull-up resistor to +5.0 V.

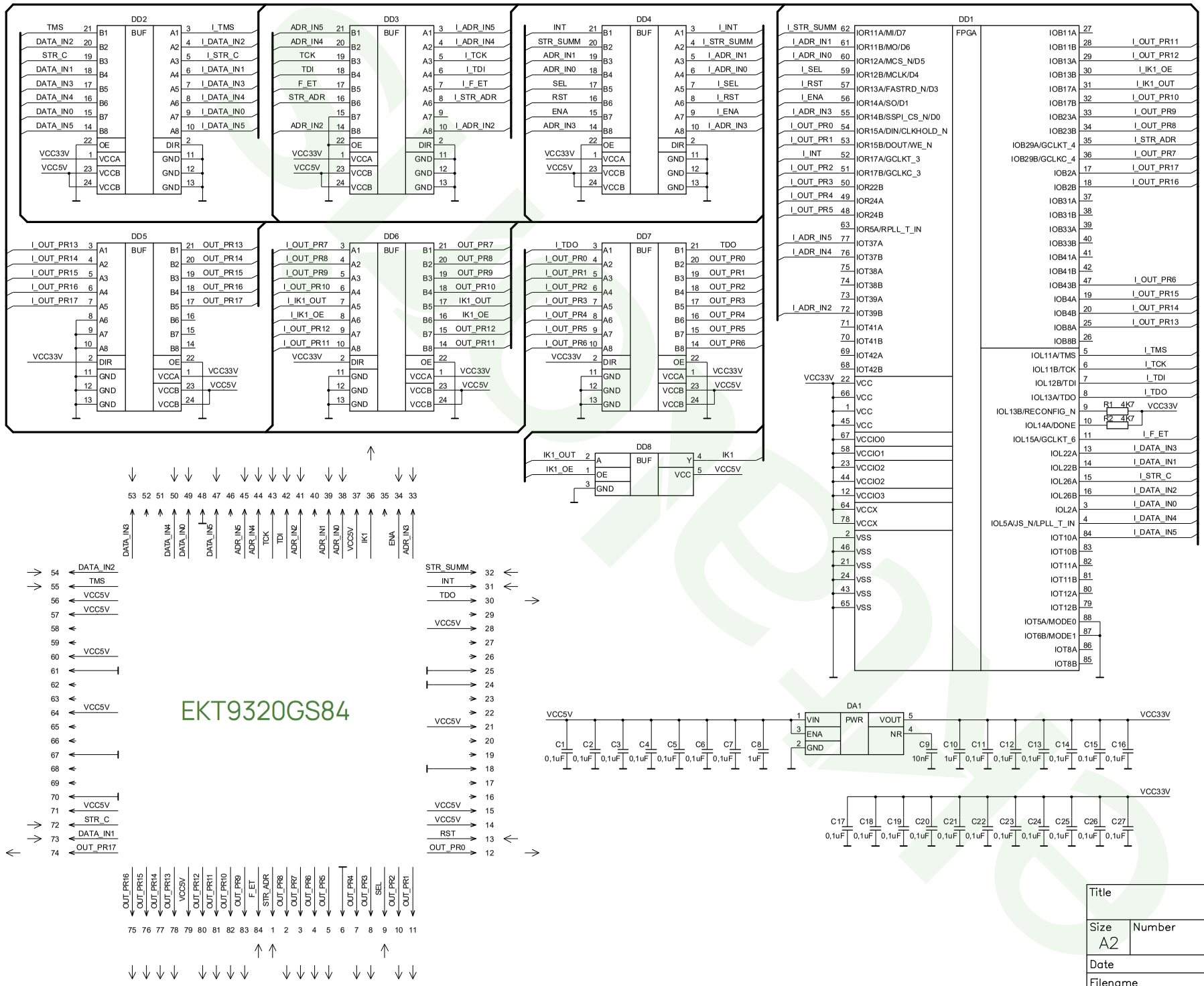
4. Operating Algorithm

The EKT9320GS84 module is a programmable pulse-width generator consisting of 18 identical channels.

To program the pulse width (phase code) of each of the 18 channels, the corresponding channel address is applied to the ADR_IN[5:0] bus. The falling edge of the STR_ADR signal then latches the pulse-width value present on the DATA_IN[5:0] bus into the internal registers.

Pulse generation is initiated on the rising edge of the INT signal when the STR_SUMM input is at a high logic level. The internal counter begins counting pulses applied to the F_ET input. When the counter value matches the programmed pulse-width value, the corresponding channel generates a pulse of the specified duration.

For external monitoring of individual channels, the channel outputs are multiplexed onto the IK1 line, which operates as a three-state output.


DD2
DD3
DD4
DD1
FPGA
DD5
DD6
DD7
DD8
EKT9320GS84
DA1
Title
Size
A2
Number
Rev
Date
Drawn by
Filename
Sheet
of