EKT7Z045 Series

Ten-million-gate-class SOPC (All-programmable system-on-chip)

Revision history

Revision	Description of changes	Revised by	Date	Notes
V1.0.0	Initial release	Xing Yanan	20250705	
V1.1.0	1. Added power supply recommendations for unused HRIO BANK VCCO. 2. Revised the product name on the cover.	Xing Yanan	20251218	
V1.2.0	1. Deleted Table 10, typical static supply current required by the device. 2. Added Section 8.2, PS power-up and power-down sequencing requirements. 3. Revised Table 22, typical static supply current required by the device.	Xing Yanan	20260119	
V1.2.1	1. Changed “Model” on the cover to “Series”. 2. Updated the company logo. 3. Removed the year from the enterprise general specification number in the ordering information note.	Tu Yikun	20260320	
V1.3.0	1. Corrected EKTSW300T to EKT7Z045 in the text. 2. Added Section 8.2, PL power-up sequencing requirements. 3. Revised Figure 3, EKT7Z045FFG900 package outline. 4. Revised Table 2, EKT7Z045FFG900 package dimensions, according to the detailed specification. 5. Revised Figure 2, EKT7Z045 typical application diagram. 6. Moved Table 21, typical static supply current required by the device, to Table 10. 7. Revised Table 11, minimum current required for device power-up. 8. Revised Table 4, terminal function descriptions.	Xing Yanan	20260401	
V1.3.1	Changed the land recommendation to the solder mask opening recommendation and added a note explaining the difference in their definitions.	Tu Yikun	20260817	

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1. Overview

The EKT7Z045 all-programmable system-on-chip is a system-on-chip (SOPC) device built on a 28nm process platform for the all-programmable market. It is positioned against the AMD (Xilinx) XC7Z045 product.

The characteristics of an all-programmable system-on-chip make it particularly suitable for applications requiring both of the following typical computing scenarios:

— High-speed, parallel, deterministic computing;
— Continuous, dynamic, non-deterministic computing.

It is primarily used in image and video processing systems that require software algorithms to extract data from images and process large numbers of pixels, including advanced driver assistance systems (ADAS), wired and wireless communications, defense and aerospace, medical endoscopy equipment, and artificial intelligence.

The product combines software programmability in the processing system (PS) with hardware programmability in the programmable logic (PL), providing excellent hardware/software coordination. EKT7Z045 incorporates an ARM Cortex-A9 MPCore dual-core processor with a clock frequency of up to 866MHz and can operate in single-processor, symmetric dual-processor and asymmetric dual-processor modes.

Table 1. EKT7Z045 product resource information

Subsystem	Resource	EKT7Z045 PBGA900 package
PS	Processor core	ARM dual-core Cortex-A9 hardware processor
PS	Processor extensions	Each processor includes a single-/double-precision floating-point unit
PS	Maximum processor frequency	866MHz
PS	L1 cache	Each processor has its own 32KB instruction cache and 32KB data cache
PS	L2 cache	512KB
PS	On-chip memory	256KB
PS	Supported external memory	DDR3, DDR3L, DDR2
PS	Supported external static memory	2 QSPI, NAND, NOR
PS	DMA channels	8
PS	Peripherals	UART, CAN, I²C, SPI, GPIO
PS	Peripherals with built-in DMA	USB, tri-speed Ethernet, SD/SDIO
PS	PS-to-PL interface	AXI interface
PS	Number of PSIO	128
PL	Logic cells	350K
PL	Look-up tables	218600
PL	Flip-flops	437200
PL	BRAM	19.2Mbits
PL	DSP	900

Table 1. EKT7Z045 product resource information (continued)

Subsystem	Resource	EKT7Z045 PBGA900 package
PL	High-speed SerDes channels (GTX)	16
PL	PCIE modules (Gen2 x8)	1
PL	High-performance user IO count	150
PL	Wide-range user IO count	212

2. Product features

EKT7Z045 consists of a processing system and programmable logic.

Processing system features

1) Dual-core ARM Cortex-A9 application processor;
2) 2.5 DMIPS/MHz per CPU;
3) Frequency up to 866MHz;
4) Timers and interrupt controllers;
5) NEON processing engine;
6) Single- and double-precision vector floating-point unit (VFPU);
7) Cache memory;
8) 32 KB L1 4-way set-associative instruction and data caches (independent for each CPU);
9) 512 KB L2 8-way set-associative cache (shared between CPUs);
10) Supports byte parity checking;
11) On-chip memory;
12) On-chip boot ROM;
13) 256KB on-chip RAM (OCM);
14) Supports byte parity checking;
15) External memory interface;
16) Supports 16-bit and 32-bit DDR3, DDR3L memory;
17) Supports 16-bit ECC mode;
18) Multi-protocol dynamic memory controller;
19) 8-channel DMA controller;
20) Supports memory-to-memory, memory-to-peripheral, peripheral-to-memory and scatter-gather modes;
21) I/O peripherals and interfaces;
22) 128 I/O;
23) Supports dual 10/100/1000 tri-speed Ethernet MAC peripherals;
24) Supports dual 12-bit analog-to-digital converters (XADC) with conversion rates up to 1MSPS;

Processing system features (continued)

25) Supports dual CAN bus interfaces compliant with CAN 2.0B;
26) Supports dual SD/SDIO 2.0/MMC3.31 controllers;
27) Supports dual full-duplex SPI ports with three peripheral chip selects;
28) Supports dual high-speed UART, up to 1Mb/s;
29) Supports dual master/slave I2C interfaces;
30) 54-bit multiplexed I/O; the I/O count can be expanded through the PL;
31) Interconnect architecture;
32) High-bandwidth interconnect within the PS and between PS and PL;
33) Interconnect based on the ARM AMBA AXI protocol;
34) Supports QoS for latency and bandwidth control.

Programmable logic features

1) Logic is implemented using 6-input look-up tables (configurable as distributed RAM);
2) On-chip data buffer block RAM has a capacity of 36Kb per block, dual-port mode and built-in FIFO;
3) User IO supports multiple single-ended signaling standards such as LVCMOS and LVTTL and multiple differential signaling standards. The voltage range of high-performance IO (HPIO) is 1.2V~1.8V, and that of wide-range IO (HRIO) is 1.2V~3.3V;
4) The high-performance user IO interface supports DDR3 at rates up to 1600Mb/s;
5) The DSP module includes a 25×18 multiplier, 48-bit accumulator and pre-adder, and can be used for high-performance filtering algorithms, such as optimal symmetric coefficient filtering;
6) High-precision, low-jitter clock management tile (CMT), including a phase-locked loop (PLL) and mixed-mode clock management (MMCM). The maximum clock management module input frequency is 800 MHz;
7) The maximum global clock tree frequency is 625MHz;
8) High-speed serial interface SerDes module with line rates from 500Mb/s up to 12.5Gb/s;
9) Integrated PCIe hard core supporting Gen2 x8;
10) Integrated 12-bit 1MSPS ADC for monitoring on-chip temperature and voltage sensors;
11) Supports multiple configuration modes, including a general-purpose memory interface and 256-bit AES encryption.

3. Functional block diagram

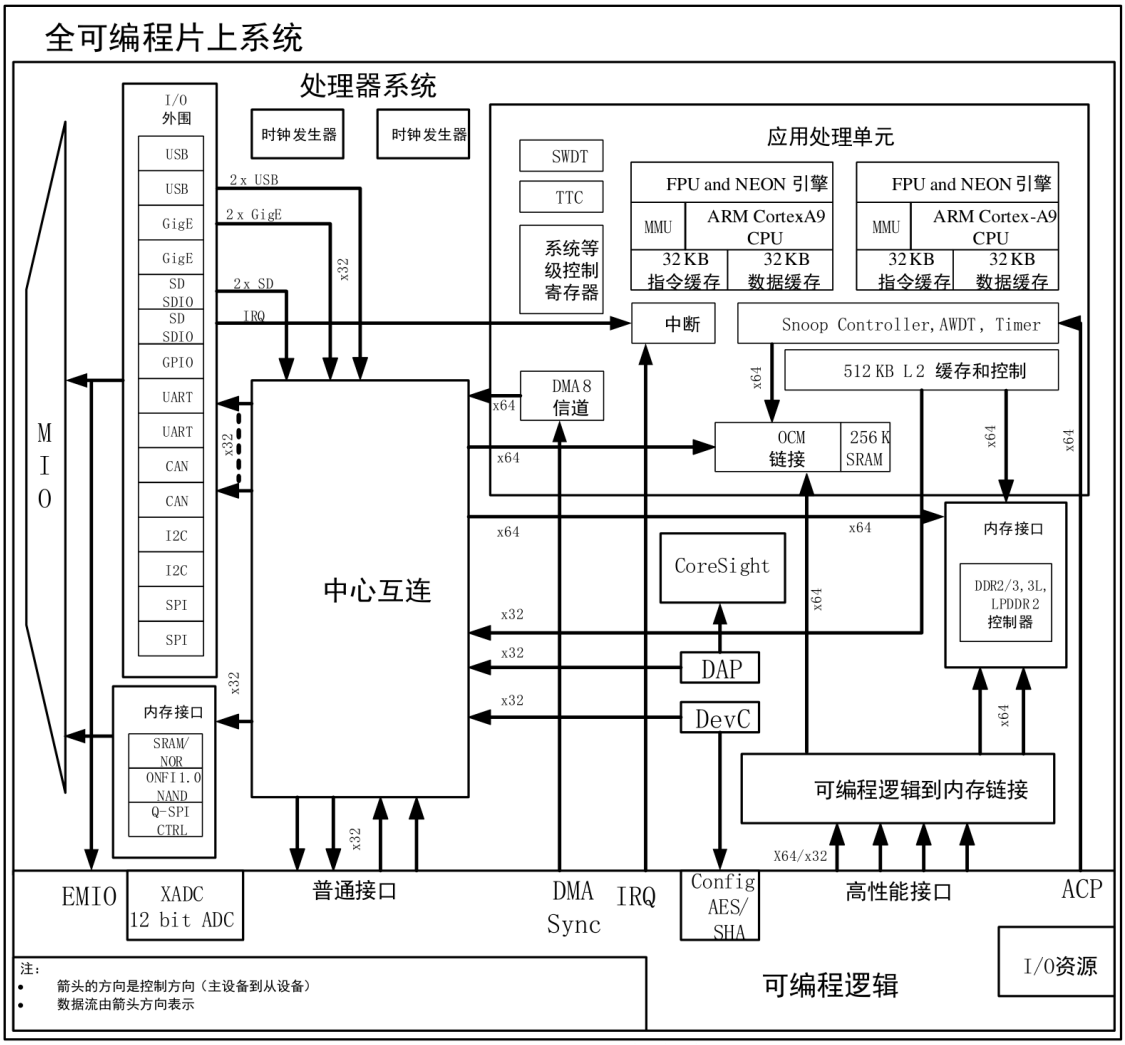


Figure 1. EKT7Z045 architecture block diagram

Diagram labels (English): All-programmable system-on-chip; Processing system; I/O peripherals; Clock generator; Application processing unit; System-level control registers; Instruction cache; Data cache; Interrupt; DMA 8 channels; L2 cache and control; OCM link; Central interconnect; Memory interface; Controller; Programmable logic-to-memory link; General-purpose interface; High-performance interface; Programmable logic; I/O resources.

Note: Arrow direction indicates control direction (master to slave). Data flow is indicated by the direction of the arrows.

Typical application scenarios for EKT7Z045 are shown in the following figure.

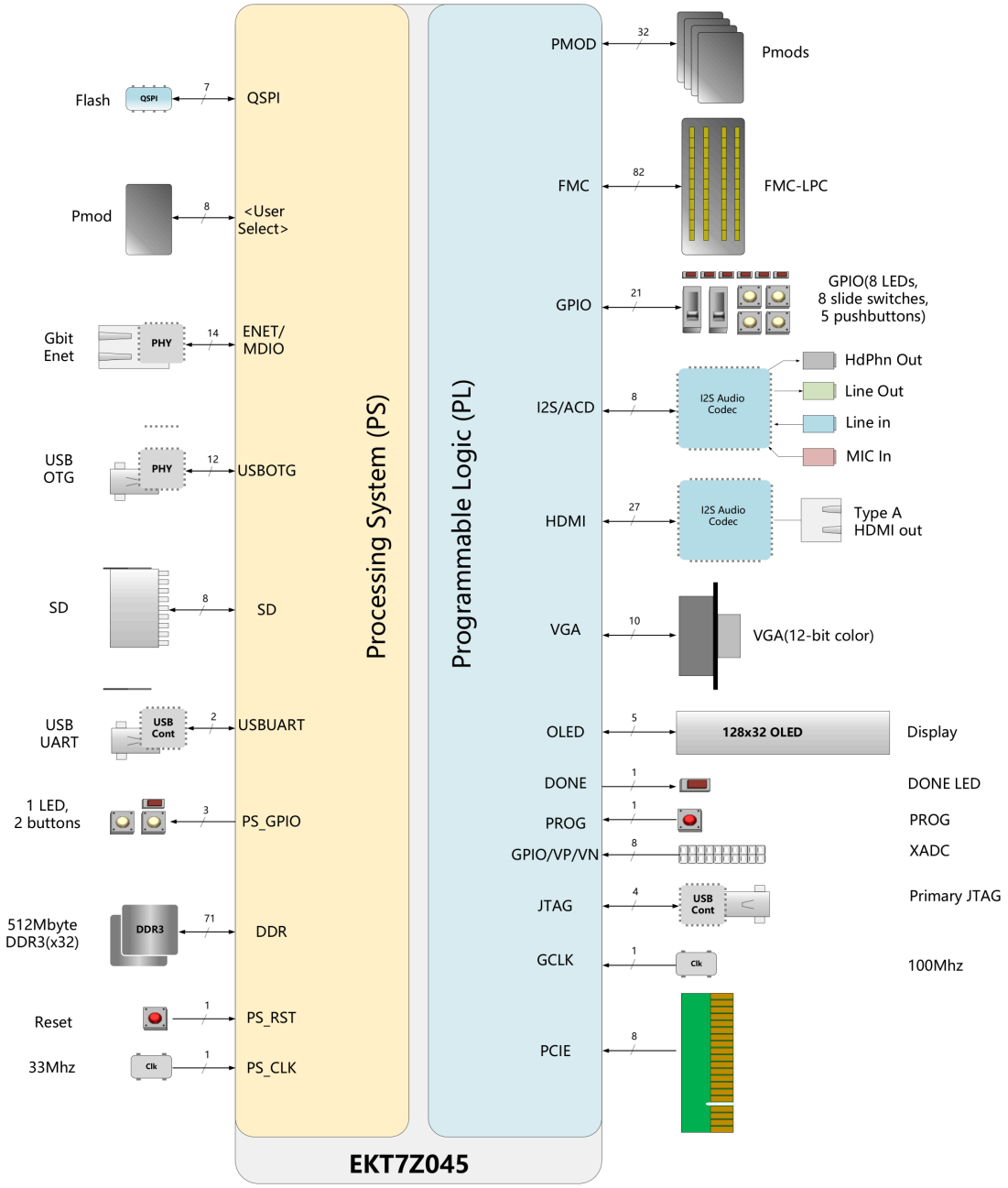


Figure 2. EKT7Z045 typical application diagram

4. Package information

4.1 Package information

EKT7Z045FFG900 uses a 900-terminal plastic package (PBGA900). The product outline dimensions are shown in the following figure.

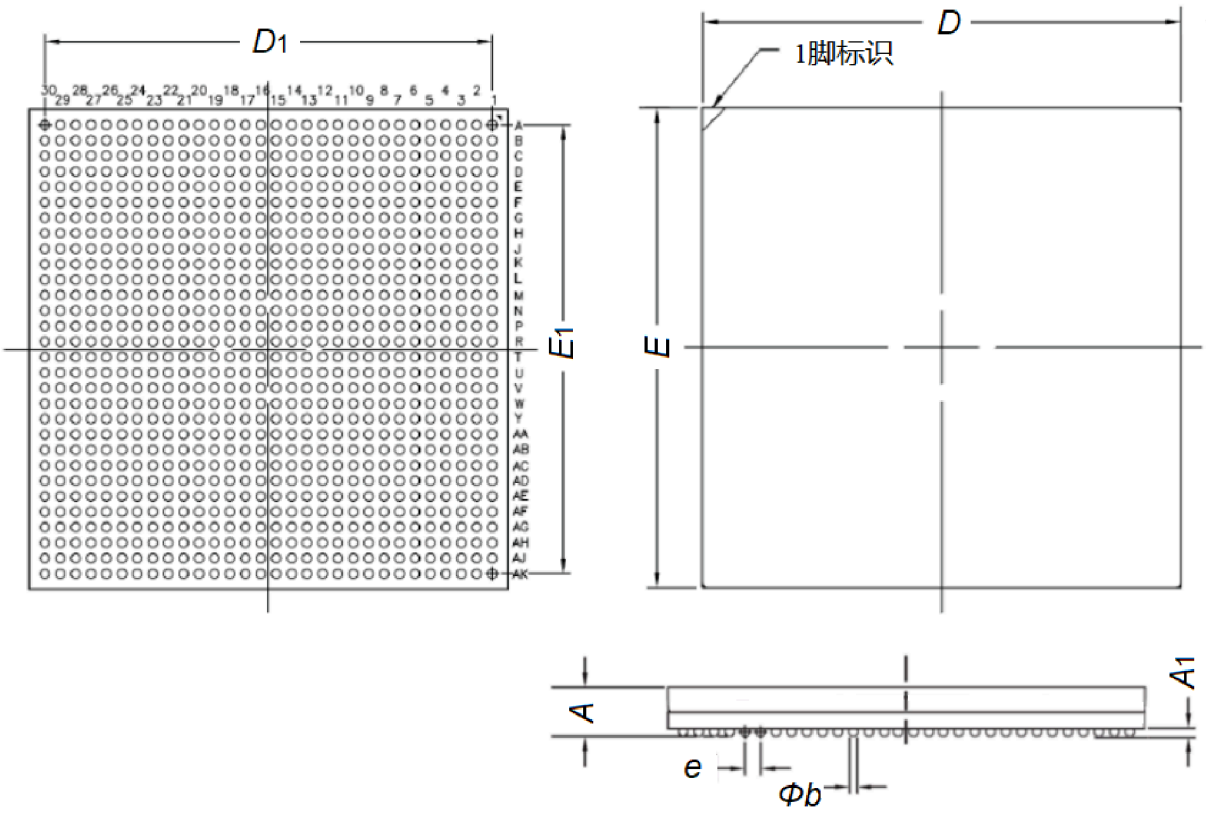


Figure 3. EKT7Z045FFG900 package outline drawing

Pin 1 identification mark.

Table 2. EKT7Z045FFG900 package dimensions (unit: mm)

Dimension symbol	Minimum	Nominal	Maximum
D/E	30.80	—	31.20
D1/E1	—	29.00	—
e	—	1.00	—
Φb	0.45	—	0.75
A1	0.33	—	0.63
A	3.12	—	3.67

The EKT7Z045FFG900 pin descriptions are shown in the following table.

Table 3. EKT7Z045FFG900 pin descriptions

Pin	Pin name	Pin	Pin name
U14	DXN_0	N8	MGTREFCLK0P_112

Table 3. EKT7Z045FFG900 pin descriptions (continued)

Pin	Pin name	Pin	Pin name
P15	VCCADC_0	T5	MGTXRXN2_112
P14	GNDADC_0	AB10	MGTAVTTRCAL_112
U15	DXP_0	N7	MGTREFCLK0N_112
R14	VREFN_0	AB9	MGTRREF_112
T15	VREFP_0	R7	MGTREFCLK1N_112
R15	VP_0	R8	MGTREFCLK1P_112
T14	VN_0	R4	MGTXTXP1_112
P9	VCCBATT_0	U4	MGTXRXP1_112
AA12	RSVDGND	R3	MGTXTXN1_112
Y12	TCK_0	U3	MGTXRXN1_112
V10	TMS_0	T2	MGTXTXP0_112
Y10	TDO_0	V6	MGTXRXP0_112
P10	TDI_0	T1	MGTXTXN0_112
W9	INIT_B_0	V5	MGTXRXN0_112
Y9	PROGRAM_B_0	D21	PS_POR_B_500
V9	CFGBVS_0	A22	PS_CLK_500
AA9	DONE_0	F24	PS_MIO0_500
U9	RSVDVCC1	D23	PS_MIO1_500
R9	RSVDVCC3	F23	PS_MIO2_500
T9	RSVDVCC2	C23	PS_MIO3_500
Y20	IO_L6P_T0_9	E23	PS_MIO4_500
AA20	IO_L6N_T0_VREF_9	C24	PS_MIO5_500
AC18	IO_L11P_T1_SRCC_9	D24	PS_MIO6_500
AC19	IO_L11N_T1_SRCC_9	B24	PS_MIO7_500
AD18	IO_L12P_T1_MRCC_9	C21	PS_MIO8_500
AD19	IO_L12N_T1_MRCC_9	A24	PS_MIO9_500
AA18	IO_L13P_T2_MRCC_9	E22	PS_MIO10_500
AA19	IO_L13N_T2_MRCC_9	A23	PS_MIO11_500
AB19	IO_L14P_T2_SRCC_9	E21	PS_MIO12_500
AB20	IO_L14N_T2_SRCC_9	F22	PS_MIO13_500
AD20	IO_L19P_T3_9	B22	PS_MIO14_500
AE20	IO_L19N_T3_VREF_9	C22	PS_MIO15_500
AA13	IO_0_10	C18	PS_MIO53_501
AK13	IO_L1P_T0_10	D19	PS_MIO52_501
AK12	IO_L1N_T0_10	F19	PS_MIO51_501
AH18	IO_L2P_T0_10	A19	PS_MIO50_501
AJ18	IO_L2N_T0_10	D18	PS_MIO49_501
AJ14	IO_L3P_T0_DQS_10	C19	PS_MIO48_501
AJ13	IO_L3N_T0_DQS_10	A18	PS_MIO47_501
AJ16	IO_L4P_T0_10	F20	PS_MIO46_501
AK16	IO_L4N_T0_10	H18	PS_MIO45_501
AJ15	IO_L5P_T0_10	E20	PS_MIO44_501

Table 3. EKT7Z045FFG900 pin descriptions (continued)

Pin	Pin name	Pin	Pin name
AK15	IO_L5N_T0_10	E18	PS_MIO43_501
AH17	IO_L6P_T0_10	D20	PS_MIO42_501
AH16	IO_L6N_T0_VREF_10	J18	PS_MIO41_501
AE12	IO_L7P_T1_10	B20	PS_MIO40_501
AF12	IO_L7N_T1_10	F18	PS_MIO39_501
AH14	IO_L8P_T1_10	A20	PS_MIO38_501
AH13	IO_L8N_T1_10	B21	PS_MIO37_501
AD14	IO_L9P_T1_DQS_10	H17	PS_MIO36_501
AD13	IO_L9N_T1_DQS_10	G21	PS_MIO35_501
AG12	IO_L10P_T1_10	K18	PS_MIO34_501
AH12	IO_L10N_T1_10	G22	PS_MIO33_501
AE13	IO_L11P_T1_SRCC_10	K17	PS_MIO32_501
AF13	IO_L11N_T1_SRCC_10	H21	PS_MIO31_501
AF14	IO_L12P_T1_MRCC_10	L18	PS_MIO30_501
AG14	IO_L12N_T1_MRCC_10	H22	PS_MIO29_501
AG17	IO_L13P_T2_MRCC_10	L17	PS_MIO28_501
AG16	IO_L13N_T2_MRCC_10	G20	PS_MIO27_501
AF15	IO_L14P_T2_SRCC_10	M17	PS_MIO26_501
AG15	IO_L14N_T2_SRCC_10	G19	PS_MIO25_501
AF18	IO_L15P_T2_DQS_10	M19	PS_MIO24_501
AF17	IO_L15N_T2_DQS_10	J21	PS_MIO23_501
AE16	IO_L16P_T2_10	L20	PS_MIO22_501
AE15	IO_L16N_T2_10	J19	PS_MIO21_501
AE18	IO_L17P_T2_10	M20	PS_MIO20_501
AE17	IO_L17N_T2_10	J20	PS_MIO19_501
AD16	IO_L18P_T2_10	K20	PS_MIO18_501
AD15	IO_L18N_T2_10	K21	PS_MIO17_501
AC14	IO_L19P_T3_10	L19	PS_MIO16_501
AC13	IO_L19N_T3_VREF_10	B19	PS_SRST_B_501
AA15	IO_L20P_T3_10	H19	PS_MIO_VREF_501
AA14	IO_L20N_T3_10	F25	PS_DDR_DRST_B_502
AB12	IO_L21P_T3_DQS_10	E25	PS_DDR_DQ1_502
AC12	IO_L21N_T3_DQS_10	A25	PS_DDR_DQ0_502
AB15	IO_L22P_T3_10	D25	PS_DDR_DQ3_502
AB14	IO_L22N_T3_10	B27	PS_DDR_DQ2_502
AC17	IO_L23P_T3_10	C27	PS_DDR_DM0_502
AC16	IO_L23N_T3_10	B26	PS_DDR_DQS_N0_502
AB17	IO_L24P_T3_10	C26	PS_DDR_DQS_P0_502
AB16	IO_L24N_T3_10	E26	PS_DDR_DQ5_502
AA17	IO_25_10	B25	PS_DDR_DQ4_502
W23	IO_0_11	E27	PS_DDR_DQ7_502
AJ25	IO_L1P_T0_11	D26	PS_DDR_DQ6_502

Table 3. EKT7Z045FFG900 pin descriptions (continued)

Pin	Pin name	Pin	Pin name
AK25	IO_L1N_T0_11	A27	PS_DDR_DQ9_502
AK22	IO_L2P_T0_11	A29	PS_DDR_DQ8_502
AK23	IO_L2N_T0_11	A28	PS_DDR_DQ11_502
AJ21	IO_L3P_T0_DQS_11	A30	PS_DDR_DQ10_502
AK21	IO_L3N_T0_DQS_11	B30	PS_DDR_DM1_502
AJ23	IO_L4P_T0_11	B29	PS_DDR_DQS_N1_502
AJ24	IO_L4N_T0_11	C29	PS_DDR_DQS_P1_502
AH23	IO_L5P_T0_11	D30	PS_DDR_DQ13_502
AH24	IO_L5N_T0_11	C28	PS_DDR_DQ12_502
AG22	IO_L6P_T0_11	D29	PS_DDR_DQ15_502
AH22	IO_L6N_T0_VREF_11	D28	PS_DDR_DQ14_502
AC24	IO_L7P_T1_11	H23	PS_DDR_A13_502
AD24	IO_L7N_T1_11	J24	PS_DDR_A14_502
AG24	IO_L8P_T1_11	H24	PS_DDR_A11_502
AG25	IO_L8N_T1_11	K23	PS_DDR_A12_502
AF23	IO_L9P_T1_DQS_11	J23	PS_DDR_A9_502
AF24	IO_L9N_T1_DQS_11	G26	PS_DDR_A10_502
AD21	IO_L10P_T1_11	K22	PS_DDR_A7_502
AE21	IO_L10N_T1_11	F27	PS_DDR_A8_502
AD23	IO_L11P_T1_SRCC_11	G24	PS_DDR_A5_502
AE23	IO_L11N_T1_SRCC_11	H26	PS_DDR_A6_502
AE22	IO_L12P_T1_MRCC_11	G25	PS_DDR_A3_502
AF22	IO_L12N_T1_MRCC_11	J26	PS_DDR_A4_502
AG21	IO_L13P_T2_MRCC_11	M21	PS_DDR_VRP_502
AH21	IO_L13N_T2_MRCC_11	N21	PS_DDR_VRN_502
AF20	IO_L14P_T2_SRCC_11	K25	PS_DDR_CKP_502
AG20	IO_L14N_T2_SRCC_11	J25	PS_DDR_CKN_502
AJ20	IO_L15P_T2_DQS_11	L27	PS_DDR_A2_502
AK20	IO_L15N_T2_DQS_11	K26	PS_DDR_A1_502
AK17	IO_L16P_T2_11	L25	PS_DDR_A0_502
AK18	IO_L16N_T2_11	M25	PS_DDR_BA2_502
AH19	IO_L17P_T2_11	M26	PS_DDR_BA1_502
AJ19	IO_L17N_T2_11	M27	PS_DDR_BA0_502
AF19	IO_L18P_T2_11	L23	PS_DDR_ODT_502
AG19	IO_L18N_T2_11	N22	PS_DDR_CS_B_502
AB21	IO_L19P_T3_11	M22	PS_DDR_CKE_502
AB22	IO_L19N_T3_VREF_11	N23	PS_DDR_WE_B_502
W21	IO_L20P_T3_11	M24	PS_DDR_CAS_B_502
Y21	IO_L20N_T3_11	N24	PS_DDR_RAS_B_502
Y22	IO_L21P_T3_DQS_11	H27	PS_DDR_DQ16_502
Y23	IO_L21N_T3_DQS_11	G27	PS_DDR_DQ17_502
AA24	IO_L22P_T3_11	H28	PS_DDR_DQ18_502

Table 3. EKT7Z045FFG900 pin descriptions (continued)

Pin	Pin name	Pin	Pin name
AB24	IO_L22N_T3_11	E28	PS_DDR_DQ19_502
AA22	IO_L23P_T3_11	H29	PS_DDR_DM2_502
AA23	IO_L23N_T3_11	G29	PS_DDR_DQS_P2_502
AC22	IO_L24P_T3_11	F29	PS_DDR_DQS_N2_502
AC23	IO_L24N_T3_11	E30	PS_DDR_DQ20_502
AC21	IO_25_11	F28	PS_DDR_DQ21_502
Y25	IO_0_12	G30	PS_DDR_DQ22_502
Y30	IO_L1P_T0_12	F30	PS_DDR_DQ23_502
AA30	IO_L1N_T0_12	J29	PS_DDR_DQ24_502
AB29	IO_L2P_T0_12	K27	PS_DDR_DQ25_502
AB30	IO_L2N_T0_12	J30	PS_DDR_DQ26_502
Y26	IO_L3P_T0_DQS_12	J28	PS_DDR_DQ27_502
Y27	IO_L3N_T0_DQS_12	K28	PS_DDR_DM3_502
Y28	IO_L4P_T0_12	L28	PS_DDR_DQS_P3_502
AA29	IO_L4N_T0_12	L29	PS_DDR_DQS_N3_502
AA27	IO_L5P_T0_12	K30	PS_DDR_DQ28_502
AA28	IO_L5N_T0_12	M29	PS_DDR_DQ29_502
AB25	IO_L6P_T0_12	L30	PS_DDR_DQ30_502
AB26	IO_L6N_T0_VREF_12	M30	PS_DDR_DQ31_502
AC26	IO_L7P_T1_12	AA6	MGTAVCC
AD26	IO_L7N_T1_12	AB8	MGTAVCC
AD30	IO_L8P_T1_12	AC10	MGTAVCC
AE30	IO_L8N_T1_12	AC6	MGTAVCC
AC29	IO_L9P_T1_DQS_12	AD8	MGTAVCC
AD29	IO_L9N_T1_DQS_12	AE10	MGTAVCC
AD25	IO_L10P_T1_12	AE6	MGTAVCC
AE26	IO_L10N_T1_12	AF8	MGTAVCC
AB27	IO_L11P_T1_SRCC_12	AG10	MGTAVCC
AC27	IO_L11N_T1_SRCC_12	AH8	MGTAVCC
AC28	IO_L12P_T1_MRCC_12	AJ10	MGTAVCC
AD28	IO_L12N_T1_MRCC_12	N6	MGTAVCC
AE28	IO_L13P_T2_MRCC_12	P8	MGTAVCC
AF28	IO_L13N_T2_MRCC_12	R6	MGTAVCC
AE27	IO_L14P_T2_SRCC_12	U6	MGTAVCC
AF27	IO_L14N_T2_SRCC_12	W6	MGTAVCC
AF29	IO_L15P_T2_DQS_12	Y8	MGTAVCC
AG29	IO_L15N_T2_DQS_12	AA2	MGTAVTT
AF30	IO_L16P_T2_12	AB4	MGTAVTT
AG30	IO_L16N_T2_12	AC2	MGTAVTT
AG26	IO_L17P_T2_12	AD4	MGTAVTT
AG27	IO_L17N_T2_12	AE2	MGTAVTT
AE25	IO_L18P_T2_12	AF4	MGTAVTT

Table 3. EKT7Z045FFG900 pin descriptions (continued)

Pin	Pin name	Pin	Pin name
AF25	IO_L18N_T2_12	AG2	MGTAVTT
AH28	IO_L19P_T3_12	AG6	MGTAVTT
AH29	IO_L19N_T3_VREF_12	AH4	MGTAVTT
AJ30	IO_L20P_T3_12	AJ2	MGTAVTT
AK30	IO_L20N_T3_12	AJ6	MGTAVTT
AJ28	IO_L21P_T3_DQS_12	AK4	MGTAVTT
AJ29	IO_L21N_T3_DQS_12	AK8	MGTAVTT
AK27	IO_L22P_T3_12	N2	MGTAVTT
AK28	IO_L22N_T3_12	P4	MGTAVTT
AH26	IO_L23P_T3_12	R2	MGTAVTT
AH27	IO_L23N_T3_12	T4	MGTAVTT
AJ26	IO_L24P_T3_12	U2	MGTAVTT
AK26	IO_L24N_T3_12	V4	MGTAVTT
AA25	IO_25_12	W2	MGTAVTT
U21	IO_0_13	Y4	MGTAVTT
P30	IO_L1P_T0_13	T7	MGTVCCAUX
R30	IO_L1N_T0_13	V7	MGTVCCAUX
T30	IO_L2P_T0_13	A1	GND
U30	IO_L2N_T0_13	A11	GND
N28	IO_L3P_T0_DQS_13	A21	GND
P28	IO_L3N_T0_DQS_13	AA1	GND
N29	IO_L4P_T0_13	AA10	GND
P29	IO_L4N_T0_13	AA11	GND
T29	IO_L5P_T0_13	AA21	GND
U29	IO_L5N_T0_13	AA5	GND
R28	IO_L6P_T0_13	AB11	GND
T28	IO_L6N_T0_VREF_13	AB18	GND
V28	IO_L7P_T1_13	AB28	GND
V29	IO_L7N_T1_13	AB3	GND
W29	IO_L8P_T1_13	AB7	GND
W30	IO_L8N_T1_13	AC1	GND
V27	IO_L9P_T1_DQS_13	AC11	GND
W28	IO_L9N_T1_DQS_13	AC15	GND
W25	IO_L10P_T1_13	AC25	GND
W26	IO_L10N_T1_13	AC5	GND
U25	IO_L11P_T1_SRCC_13	AC9	GND
V26	IO_L11N_T1_SRCC_13	AD11	GND
U26	IO_L12P_T1_MRCC_13	AD12	GND
U27	IO_L12N_T1_MRCC_13	AD22	GND
R25	IO_L13P_T2_MRCC_13	AD3	GND
R26	IO_L13N_T2_MRCC_13	AD7	GND
R27	IO_L14P_T2_SRCC_13	AE1	GND

Table 3. EKT7Z045FFG900 pin descriptions (continued)

Pin	Pin name	Pin	Pin name
T27	IO_L14N_T2_SRCC_13	AE11	GND
N26	IO_L15P_T2_DQS_13	AE19	GND
N27	IO_L15N_T2_DQS_13	AE29	GND
P25	IO_L16P_T2_13	AE5	GND
P26	IO_L16N_T2_13	AE9	GND
T24	IO_L17P_T2_13	AF11	GND
T25	IO_L17N_T2_13	AF16	GND
P23	IO_L18P_T2_13	AF26	GND
P24	IO_L18N_T2_13	AF3	GND
P21	IO_L19P_T3_13	AF7	GND
R21	IO_L19N_T3_VREF_13	AG1	GND
T22	IO_L20P_T3_13	AG11	GND
T23	IO_L20N_T3_13	AG13	GND
R22	IO_L21P_T3_DQS_13	AG23	GND
R23	IO_L21N_T3_DQS_13	AG5	GND
U22	IO_L22P_T3_13	AG9	GND
V22	IO_L22N_T3_13	AH11	GND
U24	IO_L23P_T3_13	AH20	GND
V24	IO_L23N_T3_13	AH3	GND
V23	IO_L24P_T3_13	AH30	GND
W24	IO_L24N_T3_13	AH7	GND
V21	IO_25_13	AJ1	GND
L5	IO_0_VRN_33	AJ11	GND
J4	IO_L1P_T0_33	AJ17	GND
J3	IO_L1N_T0_33	AJ27	GND
L1	IO_L2P_T0_33	AJ5	GND
K1	IO_L2N_T0_33	AJ9	GND
K3	IO_L3P_T0_DQS_33	AK11	GND
K2	IO_L3N_T0_DQS_33	AK14	GND
L3	IO_L4P_T0_33	AK24	GND
L2	IO_L4N_T0_33	AK3	GND
K5	IO_L5P_T0_33	AK7	GND
J5	IO_L5N_T0_33	B18	GND
K6	IO_L6P_T0_33	B28	GND
J6	IO_L6N_T0_VREF_33	B8	GND
G2	IO_L7P_T1_33	C15	GND
F2	IO_L7N_T1_33	C25	GND
H6	IO_L8P_T1_33	C5	GND
G6	IO_L8N_T1_33	D12	GND
J1	IO_L9P_T1_DQS_33	D2	GND
H1	IO_L9N_T1_DQS_33	D22	GND
H2	IO_L10P_T1_33	E19	GND

Table 3. EKT7Z045FFG900 pin descriptions (continued)

Pin	Pin name	Pin	Pin name
G1	IO_L10N_T1_33	E29	GND
H4	IO_L11P_T1_SRCC_33	E9	GND
H3	IO_L11N_T1_SRCC_33	F16	GND
G5	IO_L12P_T1_MRCC_33	F26	GND
G4	IO_L12N_T1_MRCC_33	F6	GND
F5	IO_L13P_T2_MRCC_33	G13	GND
E5	IO_L13N_T2_MRCC_33	G23	GND
F4	IO_L14P_T2_SRCC_33	G3	GND
F3	IO_L14N_T2_SRCC_33	H10	GND
E6	IO_L15P_T2_DQS_33	H20	GND
D5	IO_L15N_T2_DQS_33	H30	GND
D4	IO_L16P_T2_33	J17	GND
D3	IO_L16N_T2_33	J27	GND
E3	IO_L17P_T2_33	J7	GND
E2	IO_L17N_T2_33	K14	GND
E1	IO_L18P_T2_33	K24	GND
D1	IO_L18N_T2_33	K4	GND
C4	IO_L19P_T3_33	L11	GND
C3	IO_L19N_T3_VREF_33	L21	GND
B5	IO_L20P_T3_33	M1	GND
B4	IO_L20N_T3_33	M14	GND
A5	IO_L21P_T3_DQS_33	M18	GND
A4	IO_L21N_T3_DQS_33	M2	GND
C2	IO_L22P_T3_33	M28	GND
C1	IO_L22N_T3_33	M3	GND
B2	IO_L23P_T3_33	M4	GND
B1	IO_L23N_T3_33	M5	GND
A3	IO_L24P_T3_33	M6	GND
A2	IO_L24N_T3_33	M7	GND
L4	IO_25_VRP_33	M8	GND
M12	IO_0_VRN_34	M9	GND
B10	IO_L1P_T0_34	N1	GND
A10	IO_L1N_T0_34	N11	GND
B9	IO_L2P_T0_34	N13	GND
A9	IO_L2N_T0_34	N15	GND
A8	IO_L3P_T0_DQS_PUDC_B_34	N17	GND
A7	IO_L3N_T0_DQS_34	N19	GND
C7	IO_L4P_T0_34	N25	GND
B7	IO_L4N_T0_34	N5	GND
C6	IO_L5P_T0_34	N9	GND
B6	IO_L5N_T0_34	P12	GND
C9	IO_L6P_T0_34	P16	GND

Table 3. EKT7Z045FFG900 pin descriptions (continued)

Pin	Pin name	Pin	Pin name
C8	IO_L6N_T0_VREF_34	P18	GND
J11	IO_L7P_T1_34	P20	GND
H11	IO_L7N_T1_34	P22	GND
E11	IO_L8P_T1_34	P3	GND
D11	IO_L8N_T1_34	P7	GND
H12	IO_L9P_T1_DQS_34	R1	GND
G11	IO_L9N_T1_DQS_34	R11	GND
E10	IO_L10P_T1_34	R13	GND
D10	IO_L10N_T1_34	R17	GND
G10	IO_L11P_T1_SRCC_34	R19	GND
F10	IO_L11N_T1_SRCC_34	R29	GND
D9	IO_L12P_T1_MRCC_34	R5	GND
D8	IO_L12N_T1_MRCC_34	T10	GND
H9	IO_L13P_T2_MRCC_34	T12	GND
G9	IO_L13N_T2_MRCC_34	T16	GND
F9	IO_L14P_T2_SRCC_34	T18	GND
E8	IO_L14N_T2_SRCC_34	T20	GND
J8	IO_L15P_T2_DQS_34	T26	GND
H8	IO_L15N_T2_DQS_34	T3	GND
F8	IO_L16P_T2_34	T8	GND
F7	IO_L16N_T2_34	U1	GND
E7	IO_L17P_T2_34	U11	GND
D6	IO_L17N_T2_34	U13	GND
H7	IO_L18P_T2_34	U17	GND
G7	IO_L18N_T2_34	U19	GND
L7	IO_L19P_T3_34	U23	GND
K7	IO_L19N_T3_VREF_34	U5	GND
J10	IO_L20P_T3_34	V12	GND
J9	IO_L20N_T3_34	V14	GND
L8	IO_L21P_T3_DQS_34	V16	GND
K8	IO_L21N_T3_DQS_34	V18	GND
K11	IO_L22P_T3_34	V20	GND
K10	IO_L22N_T3_34	V3	GND
L10	IO_L23P_T3_34	V30	GND
L9	IO_L23N_T3_34	V8	GND
L12	IO_L24P_T3_34	W1	GND
K12	IO_L24N_T3_34	W11	GND
M10	IO_25_VRP_34	W13	GND
K16	IO_0_VRN_35	W15	GND
L15	IO_L1P_T0_AD0P_35	W17	GND
L14	IO_L1N_T0_AD0N_35	W19	GND
J13	IO_L2P_T0_AD8P_35	W27	GND

Table 3. EKT7Z045FFG900 pin descriptions (continued)

Pin	Pin name	Pin	Pin name
H13	IO_L2N_T0_AD8N_35	W5	GND
L13	IO_L3P_T0_DQS_AD1P_35	Y14	GND
K13	IO_L3N_T0_DQS_AD1N_35	Y16	GND
J14	IO_L4P_T0_35	Y18	GND
H14	IO_L4N_T0_35	Y24	GND
K15	IO_L5P_T0_AD9P_35	Y3	GND
J15	IO_L5N_T0_AD9N_35	Y7	GND
J16	IO_L6P_T0_35	M13	VCCINT
H16	IO_L6N_T0_VREF_35	M15	VCCINT
G17	IO_L7P_T1_AD2P_35	N12	VCCINT
G16	IO_L7N_T1_AD2N_35	N14	VCCINT
G15	IO_L8P_T1_AD10P_35	P13	VCCINT
G14	IO_L8N_T1_AD10N_35	R12	VCCINT
G12	IO_L9P_T1_DQS_AD3P_35	R16	VCCINT
F12	IO_L9N_T1_DQS_AD3N_35	T13	VCCINT
F13	IO_L10P_T1_AD11P_35	U12	VCCINT
E12	IO_L10N_T1_AD11N_35	U16	VCCINT
E13	IO_L11P_T1_SRCC_35	V13	VCCINT
D13	IO_L11N_T1_SRCC_35	V15	VCCINT
F15	IO_L12P_T1_MRCC_35	W12	VCCINT
F14	IO_L12N_T1_MRCC_35	W14	VCCINT
E16	IO_L13P_T2_MRCC_35	W16	VCCINT
E15	IO_L13N_T2_MRCC_35	Y17	VCCINT
D15	IO_L14P_T2_AD4P_SRCC_35	M11	VCCAUX
D14	IO_L14N_T2_AD4N_SRCC_35	N10	VCCAUX
F17	IO_L15P_T2_DQS_AD12P_35	R10	VCCAUX
E17	IO_L15N_T2_DQS_AD12N_35	U10	VCCAUX
D16	IO_L16P_T2_35	W10	VCCAUX
C16	IO_L16N_T2_35	Y11	VCCAUX
C17	IO_L17P_T2_AD5P_35	P11	VCCAUX_IO_G0
B16	IO_L17N_T2_AD5N_35	T11	VCCAUX_IO_G0
B17	IO_L18P_T2_AD13P_35	V11	VCCAUX_IO_G0
A17	IO_L18N_T2_AD13N_35	Y13	VCCO_0
C14	IO_L19P_T3_35	Y15	VCCO_0
C13	IO_L19N_T3_VREF_35	AA16	VCCO_10
C12	IO_L20P_T3_AD6P_35	AB13	VCCO_10
B12	IO_L20N_T3_AD6N_35	AD17	VCCO_10
B15	IO_L21P_T3_DQS_AD14P_35	AE14	VCCO_10
A15	IO_L21N_T3_DQS_AD14N_35	AG18	VCCO_10
C11	IO_L22P_T3_AD7P_35	AH15	VCCO_10
B11	IO_L22N_T3_AD7N_35	AJ12	VCCO_10
B14	IO_L23P_T3_35	AB23	VCCO_11

Table 3. EKT7Z045FFG900 pin descriptions (continued)

Pin	Pin name	Pin	Pin name
A14	IO_L23N_T3_35	AE24	VCCO_11
A13	IO_L24P_T3_AD15P_35	AF21	VCCO_11
A12	IO_L24N_T3_AD15N_35	AH25	VCCO_11
M16	IO_25_VRP_35	AJ22	VCCO_11
AK2	MGTXTXP3_109	AK19	VCCO_11
AE8	MGTXRXP3_109	W22	VCCO_11
AK1	MGTXTXN3_109	AA26	VCCO_12
AE7	MGTXRXN3_109	AC30	VCCO_12
AJ4	MGTXTXP2_109	AD27	VCCO_12
AG8	MGTXRXP2_109	AG28	VCCO_12
AJ3	MGTXTXN2_109	AK29	VCCO_12
AD10	MGTREFCLK0P_109	Y29	VCCO_12
AG7	MGTXRXN2_109	N30	VCCO_13
AD9	MGTREFCLK0N_109	P27	VCCO_13
AF9	MGTREFCLK1N_109	R24	VCCO_13
AF10	MGTREFCLK1P_109	T21	VCCO_13
AK6	MGTXTXP1_109	U28	VCCO_13
AJ8	MGTXRXP1_109	V25	VCCO_13
AK5	MGTXTXN1_109	B3	VCCO_33
AJ7	MGTXRXN1_109	E4	VCCO_33
AK10	MGTXTXP0_109	F1	VCCO_33
AH10	MGTXRXP0_109	H5	VCCO_33
AK9	MGTXTXN0_109	J2	VCCO_33
AH9	MGTXRXN0_109	L6	VCCO_33
AD2	MGTXTXP3_110	A6	VCCO_34
AD6	MGTXRXP3_110	C10	VCCO_34
AD1	MGTXTXN3_110	D7	VCCO_34
AD5	MGTXRXN3_110	F11	VCCO_34
AE4	MGTXTXP2_110	G8	VCCO_34
AF6	MGTXRXP2_110	J12	VCCO_34
AE3	MGTXTXN2_110	K9	VCCO_34
AA8	MGTREFCLK0P_110	A16	VCCO_35
AF5	MGTXRXN2_110	B13	VCCO_35
AA7	MGTREFCLK0N_110	D17	VCCO_35
AC7	MGTREFCLK1N_110	E14	VCCO_35
AC8	MGTREFCLK1P_110	H15	VCCO_35
AF2	MGTXTXP1_110	L16	VCCO_35
AG4	MGTXRXP1_110	AC20	VCCO_9
AF1	MGTXTXN1_110	Y19	VCCO_9
AG3	MGTXRXN1_110	V17	VCCBRAM
AH2	MGTXTXP0_110	V19	VCCBRAM
AH6	MGTXRXP0_110	W18	VCCBRAM

Table 3. EKT7Z045FFG900 pin descriptions (continued)

Pin	Pin name	Pin	Pin name
AH1	MGTXTXN0_110	W20	VCCBRAM
AH5	MGTXRXN0_110	A26	VCCO_DDR_502
V2	MGTXTXP3_111	C30	VCCO_DDR_502
AA4	MGTXRXP3_111	D27	VCCO_DDR_502
V1	MGTXTXN3_111	G28	VCCO_DDR_502
AA3	MGTXRXN3_111	H25	VCCO_DDR_502
W4	MGTXTXP2_111	K29	VCCO_DDR_502
Y6	MGTXRXP2_111	L26	VCCO_DDR_502
W3	MGTXTXN2_111	M23	VCCO_DDR_502
U8	MGTREFCLK0P_111	N20	VCCPAUX
Y5	MGTXRXN2_111	P19	VCCPAUX
U7	MGTREFCLK0N_111	R20	VCCPAUX
W7	MGTREFCLK1N_111	U20	VCCPAUX
W8	MGTREFCLK1P_111	N16	VCCPINT
Y2	MGTXTXP1_111	P17	VCCPINT
AB6	MGTXRXP1_111	R18	VCCPINT
Y1	MGTXTXN1_111	T17	VCCPINT
AB5	MGTXRXN1_111	T19	VCCPINT
AB2	MGTXTXP0_111	U18	VCCPINT
AC4	MGTXRXP0_111	N18	VCCPLL
AB1	MGTXTXN0_111	B23	VCCO_MIO0_500
AC3	MGTXRXN0_111	E24	VCCO_MIO0_500
N4	MGTXTXP3_112	F21	VCCO_MIO0_500
P6	MGTXRXP3_112	C20	VCCO_MIO1_501
N3	MGTXTXN3_112	G18	VCCO_MIO1_501
P5	MGTXRXN3_112	J22	VCCO_MIO1_501
P2	MGTXTXP2_112	K19	VCCO_MIO1_501
T6	MGTXRXP2_112	L22	PS_DDR_VREF0_502
P1	MGTXTXN2_112	L24	PS_DDR_VREF1_502

4.2 Terminal function definitions

The terminal interface signal functions are described in the following table.

Table 4. Terminal function descriptions

Pin name	Attribute	Direction	Description
PS-side ports — Functional pins			
PS_CLK	Dedicated	Input	System reference clock. PS_CLK must be between 30 MHz and 60 MHz.

Table 4. Terminal function descriptions (continued)

Pin name	Attribute	Direction	Description
PS-side ports — Functional pins (continued)			
PS_POR_B	Dedicated	Input	Power-on reset. During power-up, PS_POR_B must be held at GND until VCCPINT, VCCPAUX and VCCO_MIO0 reach the minimum operating levels, and the PS_CLK reference voltage is within specification. When PS_POR_B is set to GND, PS starts the BOOT process. During power-down, before VCCPINT reaches 0.80V, at least one of the following four conditions must be met: PS_POR_B is set to GND; The reference clock entering PS_CLK is disabled; VCCPAUX is below 0.70V; VCCO_MIO0 is below 0.90V.
PS_SRST_B	Dedicated	Input	System asynchronous reset logic. (Active low)
PS_MIO#	Multiplexed	Input / output	Can be used as multiplexed I/O for peripherals.
PS_DDR#	Dedicated	Input / output	Dedicated pins for external DDR memory control.
PS-side ports — Power / ground pins			
VCCPINT	Dedicated	N/A	PS 1.0V logic power supply, independent of the PL VCCINT supply.
VCCPAUX	Dedicated	N/A	PS 1.8V auxiliary power supply, independent of the PL VCCAUX supply.
VCCPLL	Dedicated	N/A	PS PLL 1.8V power supply. A 0.47μF to 4.7μF capacitor in a 0402 package must be placed near the VCCPLL BGA via. In addition, when powered by VCCPAUX, VCCPLL must be filtered through a 120Ω, 100MHz ferrite bead (0603 package) and a 10μF decoupling capacitor (0603 package) to minimize PLL jitter.
VCCO_MIO#	Dedicated	N/A	1.8V–3.3V PS I/O power supply for the MIO bank.
VCCO_DDR	Dedicated	N/A	1.2V–1.8V DDR I/O power supply.
PS_MIO_VREF	Dedicated	N/A	PS_MIO_VREF provides the reference voltage for the RGMII input receiver. When the RGMII interface is not used, the PS_MIO_VREF pin may be left floating. When the RGMII interface is used, connect this pin to a voltage equal to 1/2 VCCO_MIO1. For example, when using the HSTL18 RGMII interface, VCCO_MIO1 is set to 1.8V. PS_MIO_VREF must be set to 0.9V.
PS_DDR_VREF#	Dedicated	N/A	DDR reference voltage input.
PS_DDR_VRP	Dedicated	Output	Positive DDR DCI voltage reference. Used to calibrate DDR I/O drive strength. Connect to a resistor and ground it. The resistance of this resistor should be twice the DDR termination impedance and trace impedance.
PS_DDR_VRN	Dedicated	Output	Positive DDR DCI voltage reference. Used to calibrate DDR I/O drive strength. Connect to a resistor and to VCCO_DDR. The resistance of this resistor should be twice the DDR termination impedance and trace impedance.

Table 4. Terminal function descriptions (continued)

Pin name	Attribute	Direction	Description
PL-side ports — User I/O			
IO_LXXY_# IO_XX_#	User pin	Input / output	Most user I/O pins can be used as differential signals and paired. The I/O at the top and bottom of each BANK is always single-ended. User I/O pins are named in the “IO_LXXY_#” format, where: “IO” indicates a user I/O pin; “LXXY” indicates the differential pair with the unique number XX within a group (Bank). “Y” is P or N, indicating the positive or negative terminal of the differential pair, respectively; “#” indicates the group number to which the pin belongs.
PL-side ports — Configuration pins			
DONE_0	Dedicated	Bidirectional	The DONE signal indicates successful completion of configuration. (Active high)
INIT_B_0	Dedicated	Bidirectional output	Indicates initialization of the configuration memory. (Active low)
PROGRAM_B_0	Dedicated	Input	Asynchronous reset of configuration logic. (Active low)
TCK_0	Dedicated	Input	JTAG clock
TDI_0	Dedicated	Input	JTAG data input
TDO_0	Dedicated	Output	JTAG data output
TMS_0	Dedicated	Input	JTAG mode selection
CFGBVS_0	Dedicated	Input	This pin selects the pre-configuration I/O standard type for dedicated and multiplexed configuration Banks 0, 14 and 15. If VCCO of Banks 0, 14 and 15 is 2.5V or 3.3V, this pin must be connected to VCCO_0. If VCCO of Banks 0, 14 and 15 is less than or equal to 1.8V, this pin must be connected to ground. Note: To avoid device damage, this pin must be connected correctly.
PUDC_B	Multiplexed	Input	Pull-up during configuration. After power-up and during configuration, the PUDC_B input enables internal pull-up resistors on user I/O pins. (Active low) When PUDC_B is low, the internal pull-up resistor on each user I/O pin is enabled. When PUDC_B is high, the internal pull-up resistor on each user I/O pin is disabled. PUDC_B must be connected to ground or connected directly to VCCO_34 (through a resistor of 1KΩ or less).
PL-side ports — Power / ground pins			
GND	Dedicated	N/A	Ground.
VCCAUX	Dedicated	N/A	1.8V power supply support pin for auxiliary circuitry.
VCCAUX_IO_G#	Dedicated	N/A	1.8V/2.0V power supply support pin for auxiliary I/O.
VCCINT	Dedicated	N/A	0.9V/1.0V power supply support pin for internal core logic.
VCCO_#	Dedicated	N/A	Power supply support pin for output drivers (each Bank).
VCCBRAM	Dedicated	N/A	1.0V power supply support pin for PL logic block RAM.
VCCBATT_0	Dedicated	N/A	Backup power supply support for the decryption key memory. When not used, this pin should be connected to an appropriate VCC or ground.

Table 4. Terminal function descriptions (continued)

Pin name	Attribute	Direction	Description
PL-side ports — Power / ground pins (continued)			
VREF	Multiplexed	N/A	Voltage input threshold pin. When an external voltage threshold is not required, these pins become user I/O. (Each Bank)
PL-side ports — Power / ground pins — RSVD			
RSVDGND	Reserved	Input	Reserved pin; leave floating.
RSVDVCC3	Reserved	Input	Reserved pin; must be connected to VCCO_0.
RSVDVCC2	Reserved	Input	Reserved pin; must be connected to VCCO_0.
RSVDVCC1	Reserved	Input	Reserved pin; must be connected to VCCO_0.
PL-side ports — Analog-to-digital converter pins			
VCCADC_0	Dedicated	N/A	XADC analog power supply
GNDADC_0	Dedicated	N/A	XADC analog ground
VP_0	Dedicated	Input	XADC dedicated differential analog input (positive)
VN_0	Dedicated	Input	XADC dedicated differential analog input (negative)
VREFP_0	Dedicated	N/A	1.25V reference input
VREFN_0	Dedicated	N/A	1.25V reference ground
AD0P ~ AD15P AD0N ~ AD15N	Multiplexed	Input	XADC differential auxiliary analog inputs 0–15
PL-side ports — G bit (Multi-gigabit) serial transceiver pins (SERDES)			
MSERDESRXP[0:3]	Dedicated	Input	Positive terminal of the SERDES Quad differential receiver port
MSERDESRXN[0:3]	Dedicated	Input	Negative terminal of the SERDES Quad differential receiver port
MSERDESTXP[0:3]	Dedicated	Output	Positive terminal of the SERDES Quad differential transmitter port
MSERDESTXN[0:3]	Dedicated	Output	Negative terminal of the SERDES Quad differential transmitter port
MGTAVCC_G#	Dedicated	Input	1.0V analog power supply for internal transmit and receive circuitry
MGTAVTT_G#	Dedicated	Input	1.2V analog power supply for the transmit driver circuitry
MGTVCCAUX_G#	Dedicated	Input	Transmitter 1.8V auxiliary analog Quad PLL (QPLL) power supply
MGTREFCLK0/1P	Dedicated	Input	Positive terminal of the transmitter differential reference clock
MGTREFCLK0/1N	Dedicated	Input	Negative terminal of the transmitter differential reference clock
MGTAVTTRCAL	Dedicated	N/A	Provides bias current for the termination resistance calibration circuit
MGTRREF	Dedicated	Input	Reference resistance provided for the termination resistance adjustment circuit

Table 4. Terminal function descriptions (continued)

Pin name	Attribute	Direction	Description
PL-side ports — Other pins			
MRCC	Multiplexed	Input	Clock I/O used to drive BUFRs, BUFIOs, BUFGs and MMCMs/PLLs. It can also drive BUFMRs to provide multi-region BUFIO and BUFR support. When not required as a clock, it is general-purpose user I/O. When a single-ended clock is connected to a differential CC pair, it must be connected to the P terminal of the differential pair. When used in a single clock region, MRCC can drive four BUFIOs and four BUFRs in a single Bank.
SRCC	Multiplexed	Input	Clock I/O used to drive BUFRs, BUFIOs, BUFGs and MMCMs/PLLs. When not required as a clock, it is general-purpose user I/O. When a single-ended clock is connected to a differential CC pair, it must be connected to the P terminal of the differential pair. When used in a single clock region, SRCC can drive four BUFIOs and four BUFRs in a single Bank.
VRN	Dedicated	N/A	DCI voltage at the N terminal of the reference resistor (each Bank, pulled up by the reference resistor)
VRP	Dedicated	N/A	DCI voltage at the P terminal of the reference resistor (each Bank, pulled down by the reference resistor)
DXP_0, DXN_0	Dedicated	Input	Temperature-sensitive diode pins (positive DXP, negative DXN). Access the diode using DXP and DXN in Bank0. Connect to 0 when not used. To use this diode, an appropriate external thermal monitoring IC circuit must be added. Use of the internal XADC temperature sensor to monitor temperature is recommended.
T0, T1, T2, T3	Multiplexed	Input	Belong to memory byte groups 0–3.
T0_DQS, T1_DQS, T2_DQS, T3_DQS	Multiplexed	Input	DDR DQS strobe pins, belonging to memory byte groups T0–T3.

4.3 Recommended solder mask openings

Note: The solder mask opening size refers to the size of the area on the PCB side that is not covered by solder mask and is used to solder this device, rather than the size of the pad itself. Users must adjust it according to the actual application scenario.

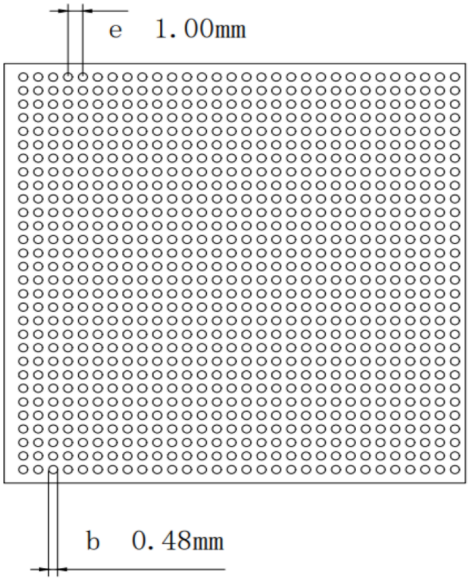


Figure 4. Recommended solder mask openings for EKT7Z045FFG900

4.4 Soldering recommendations

The v7Z045FFG900 solder ball material is Sn96.5/Ag3.0/Cu0.5 lead-free solder. The recommended reflow soldering profile is shown below.

Recommended reflow soldering conditions

Parameter	Recommendation
Reflow heating method	Hot air convection, infrared / hot air convection
Heating rate	Maximum 3°C/s
Preheat temperature 150°C–200°C	60s–120s
Time above melting point (reflow time)	60s–120s
Time within 5°C below peak temperature	Maximum 30s
Peak lead or solder ball temperature	Minimum 235°C, typical 245°C, not exceeding 260°C
Cooling rate	Maximum 6°C/s
Time from room temperature to peak temperature	Minimum 3.5 minutes, typical 5 minutes, not exceeding 8 minutes
Recommended solder paste	ALPHA OM338 SAC305
Note	Adjust accordingly based on the characteristics of the selected solder paste

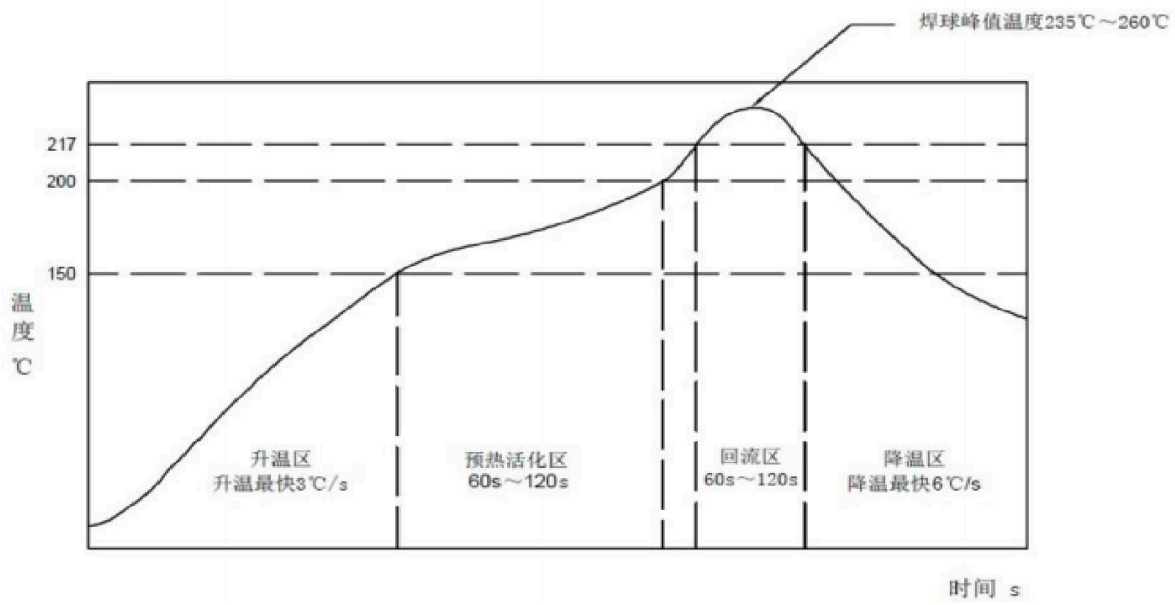


Figure 5. Recommended soldering temperature profile for EKT7Z045FFG900

Plot labels: Temperature (°C); Time (s); Solder ball peak temperature 235°C–260°C; Heating zone: maximum heating rate 3°C/s; Preheat activation zone: 60s–120s; Reflow zone: 60s–120s; Cooling zone: maximum cooling rate 6°C/s.

5. Absolute maximum ratings and recommended operating range

5.1 Absolute maximum ratings

Table 5. Absolute maximum ratings [1,2]

No.	Symbol	Description	Min.	Max.	Unit
Processing system PS					
1	V_CCPINT	Core supply	-0.5	1.1	V
2	V_CCPAUX	Auxiliary supply	-0.5	2.0	V
3	V_CCPLL	Phase-locked loop supply	-0.5	2.0	V
4	V_CCO_DDR	DDR supply	-0.5	2.0	V
5	V_CCO_MIO	MIO supply	-0.5	3.6	V
6	V_PIN	MIO IO input voltage	-0.55	VCCO_MIO+0.55	V
6	V_PIN	DDR IO input voltage	-0.4	VCCO_MIO+0.55	V
7	V_PREF	Input reference voltage	-0.5	2.0	V
Programmable logic PL					
8	V_CCINT	Core supply	-0.5	1.1	V
9	V_CCAUX	Auxiliary supply	-0.5	2.0	V
10	V_BRAM	Auxiliary user IO supply, when set to 1.8V	-0.5	2.06	V
10	V_CCO	Internal block RAM supply	-0.5	1.1	V

Table 5. Absolute maximum ratings [1,2] (continued)

No.	Symbol	Description	Min.	Max.	Unit
Programmable logic PL (continued)					
11	V_CCAUX_IO	HRIO supply	-0.5	3.6	V
12	V_CCAUX_IO	HPIO supply	-0.5	2.0	V
13	V_REF	Input reference voltage	-0.5	2.0	V
14	V_IN[3]	High-performance user IO input voltage	-0.55	VCCO+0.55	V
14	V_IN[3]	Wide-range user IO input voltage	-0.4	VCCO+0.55	V
15	V_CCBATT	Key storage backup battery voltage	-0.5	2.0	V
SERDES high-speed transceiver					
16	V_MGTAVCC	High-speed transceiver analog circuit supply	-0.5	1.1	V
17	V_MGTAVTT	High-speed transceiver termination circuit supply	-0.5	1.32	V
18	V_MGTVCCAUX	High-speed transceiver QPLL auxiliary supply	-0.5	1.935	V
19	V_MGTREFCLK	High-speed transceiver reference clock absolute input voltage	-0.5	1.32	V
20	V_MGTAVTTRCAL	High-speed transceiver resistor calibration circuit analog supply	-0.5	1.32	V
21	V_MGTIN	High-speed transceiver absolute input voltage	-0.5	1.26	V
22	I_DCIN-FLOAT	RX input pin DC-coupled input current when RX terminal is floating	--	14	mA
23	I_DCIN-MGTAVTT	RX input pin DC-coupled input current when RX terminal is VMGTAVTT	--	12	mA
24	I_DCIN-GND	RX input pin DC-coupled input current when RX terminal is GND	--	12	mA
25	I_DCOUT-FLOAT	TX output pin DC-coupled output current when RX terminal is floating	--	14	mA
26	I_DCOUT-MGTAVTT	TX output pin DC-coupled output current when RX terminal is VMGTAVTT	--	12	mA
On-chip ADC module					
27	V_CCADC	ADC supply voltage relative to GNDADC	-0.5	2.0	V
28	V_REFP	Externally supplied reference voltage relative to GNDADC	-0.5	2.0	V
Temperature range					
29	T_STG	Storage ambient temperature	-65	150	°C
30	T_SOL	Maximum soldering temperature of package terminal lead-free solder balls	--	260	°C
31	T_J	Maximum device junction temperature (military/M3 grade)	-55	125	°C
31	T_J	Maximum device junction temperature (industrial grade I)	-40	85	°C
32	θ_JC	Thermal resistance	--	0.10	°C/W

Note 1: Stresses beyond the absolute maximum ratings may cause permanent damage to the device. The table above is a stress rating only and does not imply functional operation of the device at these or any conditions beyond those specified above. Extended exposure to absolute maximum rated conditions may affect device reliability.

Note 2: The maximum ratings apply to input DC signals. See Tables 6 and 7 for the maximum overshoot and undershoot specifications for AC input signals.

Table 6. Maximum permitted AC overshoot and undershoot input voltage for user I/O (HPIO) [1,2]

No.	AC overshoot voltage (V)	% of UI	AC undershoot voltage (V)	% of UI
1	V_CCO + 0.55	100	-0.55	100
2	V_CCO + 0.60	50.0[3]	-0.60	50.0[3]
3	V_CCO + 0.65	50.0[3]	-0.65	50.0[3]
4	V_CCO + 0.70	47.0	-0.70	50.0[3]
5	V_CCO + 0.75	21.2	-0.75	50.0[3]
6	V_CCO + 0.80	9.71	-0.80	50.0[3]
7	V_CCO + 0.85	4.51	-0.85	28.4
8	V_CCO + 0.90	2.12	-0.90	12.7
9	V_CCO + 0.97	1.01	-0.97	5.79

Note 1: The total for each IO Bank must not exceed 200 mA.

Note 2: The duration of the peak overshoot or undershoot voltage above V_CCO + 0.20V or below GND - 0.20V must not exceed the values in the table above.

Note 3: UI duration is less than 20µs.

Table 7. Maximum permitted AC overshoot and undershoot input voltage for user I/O (HRIO) [1,2]

No.	AC overshoot voltage (V)	% of UI	AC undershoot voltage (V)	% of UI
1	V_CCO + 0.55	100	-0.40	100
1	V_CCO + 0.55	100	-0.45	61.7
1	V_CCO + 0.55	100	-0.50	25.8
1	V_CCO + 0.55	100	-0.55	11.0
2	V_CCO + 0.60	46.6	-0.60	4.77
3	V_CCO + 0.65	21.2	-0.65	2.10
4	V_CCO + 0.70	9.75	-0.70	0.94
5	V_CCO + 0.75	4.55	-0.75	0.43
6	V_CCO + 0.80	2.15	-0.80	0.20
7	V_CCO + 0.85	1.02	-0.85	0.09
8	V_CCO + 0.90	0.49	-0.90	0.04
9	V_CCO + 0.97	0.24	-0.97	0.02

Note 1: The total for each IO Bank must not exceed 200 mA.

Note 2: The duration of the peak overshoot or undershoot voltage above V_CCO + 0.20V or below GND - 0.20V must not exceed the values in the table above.

Table 8. Maximum permitted AC overshoot and undershoot input voltage for dedicated configuration pins [1,2]

No.	AC overshoot voltage (V)	% of UI	AC undershoot voltage (V)	% of UI
1	V_CCO + 0.55	100	-0.40	100
1	V_CCO + 0.55	100	-0.45	61.7
1	V_CCO + 0.55	100	-0.50	25.8
1	V_CCO + 0.55	100	-0.55	11.0
2	V_CCO + 0.60	46.6	-0.60	4.77
3	V_CCO + 0.65	21.2	-0.65	2.10
4	V_CCO + 0.70	9.75	-0.70	0.94
5	V_CCO + 0.75	4.55	-0.75	0.43
6	V_CCO + 0.80	2.15	-0.80	0.20
7	V_CCO + 0.85	1.02	-0.85	0.09
8	V_CCO + 0.90	0.49	-0.90	0.04
9	V_CCO + 0.97	0.24	-0.97	0.02

Note 1: The total for the dedicated configuration pin Bank must not exceed 200 mA.

Note 2: The duration of the peak overshoot or undershoot voltage above V_CCO + 0.20V or below GND - 0.20V must not exceed the values in the table above.

5.2 Recommended operating range

Table 9. Recommended operating conditions [1,2,3,4,5,6,7]

No.	Symbol	Description	Min.	Typ.	Max.	Unit
Processing system PS						
1	V_CCPINT	Core supply	0.97	1.00	1.03	V
2	V_CCPAUX	Auxiliary supply	1.71	1.80	1.89	V
3	V_CCPLL	Phase-locked loop supply	1.71	1.80	1.89	V
4	V_CCO_DDR	DDR supply	1.14	-	1.89	V
5	V_CCO_MIO	MIO supply	1.71	-	3.465	V
6	V_PIN	MIO IO input voltage	-0.2	—	V_CCO+0.2	V
6	V_PIN	DDR IO input voltage	-0.2	—	V_CCO+0.2	V
Programmable logic PL						
7	V_CCINT	Core supply	0.97	1.00	1.03	V
8	V_CCAUX	Auxiliary supply	1.71	1.80	1.89	V
9	V_CCBRAM	Internal block RAM supply	0.97	1.00	1.03	V
10	V_CCO	HRIO supply	1.14	-	3.465	V
10	V_CCO	High-performance user HPIO supply	1.14	—	1.89	V
11	V_IN	IO input voltage	-0.2	—	VCCO+0.2	V

Table 9. Recommended operating conditions [1,2,3,4,5,6,7] (continued)

No.	Symbol	Description	Min.	Typ.	Max.	Unit
Programmable logic PL (continued)						
11	V_IN	When V_CCO is 3.3V: IO input voltage for V_REF and differential standards (except TMDS33)	-0.2	—	2.625	V
12	V_CCAUX_IO	IO auxiliary supply when set to 1.8V	1.71	1.80	1.89	V
12	V_CCAUX_IO	IO auxiliary supply when set to 2.0V	1.94	2.00	2.06	V
13	V_CCBATT	Key storage backup battery voltage	1.0	-	1.89	V
High-speed serial transceiver						
14	V_MGTAVCC	High-speed transceiver QPLL analog supply voltage, QPLL frequency range ≤ 10.3125GHz	0.97	1.00	1.08	V
14	V_MGTAVCC	High-speed transceiver QPLL analog supply voltage, QPLL frequency range >10.3125GHz	1.02	1.03	1.08	V
15	V_MGTAVTT	High-speed transceiver termination circuit supply	1.17	1.20	1.23	V
16	V_MGTVCCAUX	High-speed transceiver QPLL auxiliary supply	1.75	1.80	1.85	V
17	V_MGTAVTTRCAL	High-speed transceiver resistor calibration circuit analog supply	1.17	1.20	1.23	V
On-chip ADC module						
18	V_CCADC	ADC supply voltage relative to GNDADC	1.71	1.80	1.89	V
19	V_REFP	Externally supplied reference voltage	1.20	1.25	1.30	V
Operating temperature range						
20	T_j	Device operating junction temperature	-55	—	125	°C

Note 1: PS power supplies and PL power supplies are independent.

Note 2: V_CCINT and V_CCBRAM should be connected to the same power supply.

Note 3: Even if V_CCO drops to 0V, configuration data is retained. V_CCO includes 1.2V, 1.35V, 1.5V, 1.8V, 2.5V and 3.3V ranges, ±5%.

Note 4: The total for each IO Bank must not exceed 200 mA.

Note 5: V_CCBATT is required only when bitstream encryption is used. If no battery is used, connect V_CCBATT to ground or V_CCAUX.

Note 6: Each listed voltage requires the filter circuit described in the product application manual for this device.

Note 7: V_MGTAVTT and V_MGTAVTTRCAL are shorted together for use.

Table 10. Typical static supply current required by the device

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V, V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V. IO resources selected for single-ended operating mode; device has a blank configuration, no output current load, no active input pull-up resistors, and all I/O pins are tri-stated and floating.

Characteristic	Symbol	Min.	Max.	Unit
V_CCPINT static supply current	I_CCPINTQ	—	1000	mA
V_CCPAUX static supply current	I_CCPAUXQ		50	mA

Table 10. Typical static supply current required by the device (continued)

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V, V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V. IO resources selected for single-ended operating mode; device has a blank configuration, no output current load, no active input pull-up resistors, and all I/O pins are tri-stated and floating.

Characteristic	Symbol	Min.	Max.	Unit
V_CCPLL static supply current	I_CCPLLQ		50	mA
V_CCINT static supply current	I_CCINTQ	—	4000	mA
V_CCAUX static supply current	I_CCAUXQ	—	600	mA
V_CCADC static supply current	I_CCADCQ		50	mA
V_CCO static supply current	I_CCOQ	—	50	mA
V_CCBRAM static supply current	I_CCBRAMQ	—	250	mA

Table 11. Minimum current required for device power-up — EKT7Z045

Current symbol	Required current	Unit
I_CCPINTMIN	I_CCPINTQ + 70	mA
I_CCPAUX	I_CCPAUX + 40	mA
I_CCDDRMIN	I_CCDDRQ + 130 per bank	mA
I_CCINTMIN	I_CCINTQ + 1400	mA
I_CCAUXMIN	I_CCAUXQ + 60	mA
I_CCOMIN	I_CCOQ + 90 mA /IO Bank	mA
I_CCAUX_IOMIN	I_CCOAUXIOQ + 40 mA /IO Bank	mA
I_CCBRAMMIN	I_CCBRAMQ + 90	mA

Table 12. Device power-up rise time [1,2,3]

No.	Symbol	Description	Condition	Min.	Max.	Unit
1	t_VCCINT[1]	Rise time from GND to 90% of V_CCPINT		0.2	50	ms
2	t_VCCPAUX	Rise time from GND to 90% of V_CCPAUX		0.2	50	ms
3	t_VCCO_DDR	Rise time from GND to 90% of V_CCO_DDR		0.2	50	ms
4	t_VCCO_MIO	Rise time from GND to 90% of V_CCO_MIO		0.2	50	ms
5	t_VCCINT	Rise time from GND to 90% of V_CCINT	--	0.2	50	ms
6	t_VCCO	Rise time from GND to 90% of V_CCO	--	0.2	50	ms
7	t_VCCAUX	Rise time from GND to 90% of V_CCAUX	--	0.2	50	ms
8	t_VCCAUX_IO	Rise time from GND to 90% of V_CCAUX_IO	--	0.2	50	ms
9	t_VCCBRAM	Rise time from GND to 90% of V_CCBRAM	--	0.2	50	ms
10	t_MGTAVCC[2]	Rise time from GND to 90% of V_MGTAVCC	--	0.2	50	ms
11	t_MGTAVTT	Rise time from GND to 90% of V_MGTAVTT	--	0.2	50	ms
12	t_MGTVCCAUX	Rise time from GND to 90% of V_MGTVCCAUX	--	0.2	50	ms

Note 1: PS and PL power supplies are completely independent, so there is no power-up sequence requirement between the supplies on the two sides.

Note 2: The recommended PS power-up sequence is VCCPINT, VCCPAUX, VCCAUX_IO, VCCPLL and PS VCCO (VCCO_MIO0, VCCO_MIO1, VCCO_DDR) to achieve minimum current consumption during power-up and ensure IO is tri-stated. The recommended power-down sequence is the reverse of the recommended power-up sequence. The PS_POR_B port must be held at GND until power-up is complete.

Note 3: The recommended PL power-up supply sequence is V_CCINT, V_CCBRAM, V_CCAUX and V_CCO to achieve minimum power-up current and ensure I/Os are tri-stated during power-up. The recommended power-down supply sequence is the reverse of the power-up supply sequence. If V_CCINT, VCCAUX_IO and V_CCBRAM have the same voltage value, they may be driven by the same power supply and powered up simultaneously.

6. Electrical characteristics

6.1 DC electrical characteristics

Table 13. DC electrical characteristics

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V, V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Data retention V_CCINT voltage	V_DRINT	-	0.75	—	V
Data retention V_CCAUX voltage	V_DRI	-	1.5	—	V
V_REF pin leakage current	I_REF	V_CCINT=1.03V, V_CCBRAM=1.03V, V_CCAUX=1.89V, V_CCO=1.89V, V_REF=0.9V, V_CCPINT=1.03V, V_CCPAUX=1.89V, V_CCAUX_IO=1.89V, V_CCO_DDR=1.89V, V_CCO_MIO=1.89V	—	15	µA
Pin input or output leakage current	I_L	V_CCINT=1.03V, V_CCBRAM=1.03V, V_CCAUX=1.89V, V_CCO=1.89V, V_CCAUX_IO=1.89V	—	15	µA
Pin pull-up current	I_RPU	Pin pull-up enabled, V_IN=0V, V_CCO=3.3V, V_CCINT=1.00V, V_CCBRAM=1.00V, V_CCAUX=1.80V, V_CCAUX_IO=1.80V	80	330	µA
Pin pull-up current	I_RPU	Pin pull-up enabled, V_IN=0V, V_CCO=1.8V, V_CCAUX_IO=1.80V, V_CCINT=1.00V, V_CCBRAM=1.00V, V_CCAUX=1.80V	34	220	µA
Pin pull-up current	I_RPU	Pin pull-up enabled, V_IN=0V, V_CCO=1.2V, V_CCINT=1.00V, V_CCBRAM=1.00V, V_CCAUX=1.80V, V_CCAUX_IO=1.80V	12	120	µA
Pin pull-down current	I_RPD	Pin pull-down enabled, VIN=3.3V, V_CCO=3.3V, V_CCAUX_IO=1.80V, V_CCINT=1.00V, V_CCBRAM=1.00V, V_CCAUX=1.80V	68	330	µA
ADC analog supply current, analog circuit powered on	I_CCADC	V_CCINT=1.00V, V_CCBRAM=1.00V, V_CCAUX=1.80V, V_CCAUX_IO=1.80V, V_CCO=1.80V, V_CCADC=1.89V, V_REFP=1.25V	—	25	mA

Table 14. PS single-ended input low-level voltage

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Condition	Min.	Max.	Unit
MIO input low-level voltage — V_IL			
HSTL_I_18, V_CCO_MIO=1.8×(1±5%) V, V_PREF=V_CCO_MIO/2	-0.3	V_PREF-0.100	V
LVCMOS33, V_CCO_MIO=3.3×(1±5%) V	-0.3	0.8	V
LVCMOS25, V_CCO_MIO=2.5×(1±5%) V	-0.3	0.7	V
LVCMOS18, V_CCO_MIO=1.8×(1±5%) V	-0.3	35%×V_CCO_MIO	V

Table 15. PL single-ended input low-level voltage

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V.

Condition	Min.	Max.	Unit
Input low-level voltage — V_IL			
LVTTL, V_CCO=3.3×(1±5%) V	-0.3	0.8	V
LVCMOS33, V_CCO=3.3×(1±5%) V	-0.3	0.8	V
LVCMOS25, V_CCO=2.5×(1±5%) V	-0.3	0.7	V
LVCMOS18, V_CCO=1.8×(1±5%) V	-0.3	35%V_CCO	V
LVCMOS15, V_CCO=1.5×(1±5%) V	-0.3	35%V_CCO	V
LVCMOS12, V_CCO=1.2×(1±5%) V	-0.3	35%V_CCO	V
HSTL_II, V_CCO=1.5×(1±5%) V, V_REF=V_CCO/2	-0.3	V_REF-0.1	V
SSTL15, V_CCO=1.5×(1±5%) V, V_REF=V_CCO/2	-0.3	V_REF-0.1	V
HSTL_I_18, V_CCO=1.8×(1±5%) V, V_REF=V_CCO/2	-0.3	V_REF-0.1	V
SSTL18_I, V_CCO=1.8×(1±5%) V, V_REF=V_CCO/2	-0.3	V_REF-0.125	V
SSTL18_II, V_CCO=1.8×(1±5%) V	-0.3	V_REF-0.125	V
SSTL135, V_CCO=1.35×(1±5%) V, V_REF=V_CCO/2	-0.3	V_REF-0.09	V

Table 16. PS single-ended input high-level voltage

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Condition	Min.	Max.	Unit
MIO input high-level voltage — V_IH			
HSTL_I_18, V_CCO_MIO=1.8×(1±5%) V, V_PREF=V_CCO_MIO/2	V_PREF+0.100	V_CCO_MIO+0.3	V
LVCMOS33, V_CCO_MIO=3.3×(1±5%) V	2.0	3.450	V
LVCMOS25, V_CCO_MIO=2.5×(1±5%) V	1.7	V_CCO_MIO+0.3	V
LVCMOS18, V_CCO_MIO=1.8×(1±5%) V	65% V_CCO_MIO	V_CCO_MIO+0.3	V

Table 17. PL single-ended input high-level voltage

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V.

Condition	Min.	Max.	Unit
Input high-level voltage — V_IH			
LVCMOS18, V_CCO=1.8×(1±5%) V	65% V_CCO	V_CCO+0.3	V
LVCMOS25, V_CCO=2.5×(1±5%) V	1.7	V_CCO+0.3	V
LVCMOS33/LVTTL, V_CCO=3.3×(1±5%) V	2.0	3.450	V
LVCMOS15, V_CCO=1.5×(1±5%) V	65% V_CCO	V_CCO+0.3	V
LVCMOS12, V_CCO=1.2×(1±5%) V	65% V_CCO	V_CCO+0.3	V
HSTL_II, V_CCO=1.5×(1±5%) V, V_REF=V_CCO/2	V_REF+0.1	V_CCO+0.3	V
SSTL15, V_CCO=1.5×(1±5%) V, V_REF=V_CCO/2	V_REF+0.1	V_CCO+0.3	V
HSTL_I_18, V_CCO=1.8×(1±5%) V, V_REF=V_CCO/2	V_REF+0.1	V_CCO+0.3	V
SSTL18_I, V_CCO=1.8×(1±5%) V, V_REF=V_CCO/2	V_REF+0.125	V_CCO+0.3	V
SSTL18_II, V_CCO=1.8×(1±5%) V, V_REF=V_CCO/2	V_REF+0.125	V_CCO+0.3	V
SSTL135, V_CCO=1.35×(1±5%) V, V_REF=V_CCO/2	V_REF+0.09	V_CCO+0.3	V

Table 18. PS single-ended output low-level voltage

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Condition	Min.	Max.	Unit
MIO output low-level voltage — V_OL			
HSTL_I_18, V_CCO_MIO=1.8×(1±5%) V, V_PREF=V_CCO_MIO/2	—	0.400	V
LVCMOS33, V_CCO_MIO=3.3×(1±5%) V	—	0.400	V
LVCMOS25, V_CCO_MIO=2.5×(1±5%) V	—	0.400	V
LVCMOS18, V_CCO_MIO=1.8×(1±5%) V	—	0.450	V

Table 19. PL single-ended output low-level voltage

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V.

Condition	Min.	Max.	Unit
Output low-level voltage — V_OL			
LVCMOS18, V_CCO=1.8×(1±5%) V, I_OL=16mA	—	0.45	V
LVCMOS25, V_CCO=2.5×(1±5%) V, I_OL=16mA	—	0.4	V
LVCMOS33, V_CCO=3.3×(1±5%) V, I_OL=16mA	—	0.4	V
LVTTL, V_CCO=3.3×(1±5%) V, I_OL=24mA	—	0.4	V
LVCMOS15, V_CCO=1.5×(1±5%) V, I_OL=16mA	—	25% V_CCO	V
LVCMOS12, V_CCO=1.2×(1±5%) V, I_OL=8mA	—	0.4	V
HSTL_II, V_CCO=1.5×(1±5%) V, V_REF=V_CCO/2, I_OL=16mA	—	0.4	V
SSTL15, V_CCO=1.5×(1±5%) V, V_REF=V_CCO/2, I_OL=13mA	—	V_CCO/2-0.175	V
HSTL_I_18, V_CCO=1.8×(1±5%) V, V_REF=V_CCO/2, I_OL=8mA	—	0.4	V

Table 19. PL single-ended output low-level voltage (continued)

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V.

Condition	Min.	Max.	Unit
Output low-level voltage — V_OL (continued)			
SSTL18_I, V_CCO=1.8×(1±5%) V, V_REF=V_CCO/2, I_OL=8mA	—	V_CCO/2-0.47	V
SSTL18_II, V_CCO=1.8×(1±5%) V, V_REF=V_CCO/2, I_OL=13.4mA	—	V_CCO/2-0.6	V
SSTL135, V_CCO=1.35×(1±5%) V, V_REF=V_CCO/2, I_OL=13mA	—	V_CCO/2-0.15	V

Table 20. PS single-ended output high-level voltage

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Condition	Min.	Max.	Unit
MIO output high-level voltage — V_OH			
HSTL_I_18, V_CCO_MIO=1.8×(1±5%) V, V_PREF=V_CCO_MIO/2	V_CCO_MIO-0.400	—	V
LVCMOS33, V_CCO_MIO=3.3×(1±5%) V	V_CCO_MIO-0.400	—	V
LVCMOS25, V_CCO_MIO=2.5×(1±5%) V	V_CCO_MIO-0.400	—	V
LVCMOS18, V_CCO_MIO=1.8×(1±5%) V	V_CCO_MIO-0.450	—	V

Table 21. PL single-ended output high-level voltage

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V.

Condition	Min.	Max.	Unit
Output high-level voltage — V_OH			
LVCMOS18, V_CCO=1.8×(1±5%) V, I_OH=-16mA	V_CCO-0.45	—	V
LVCMOS25, V_CCO=2.5×(1±5%) V, I_OH=-16mA	V_CCO-0.4	—	V
LVTTL, V_CCO=3.3×(1±5%) V, I_OH=-24mA	2.4	—	V
LVCMOS33, V_CCO=3.3×(1±5%) V, I_OH=-16mA	V_CCO-0.4	—	V
LVCMOS15, V_CCO=1.5×(1±5%) V, I_OH=-16mA	75% V_CCO	—	V
LVCMOS12, V_CCO=1.2×(1±5%) V, I_OH=-8mA	V_CCO-0.4	—	V
HSTL_II, V_CCO=1.5×(1±5%) V, V_REF=V_CCO/2, I_OH=-16mA	V_CCO-0.4	—	V
SSTL15, V_CCO=1.5×(1±5%) V, V_REF=V_CCO/2, I_OH=-13mA	V_CCO/2+0.175	—	V
HSTL_I_18, V_CCO=1.8×(1±5%) V, V_REF=V_CCO/2, I_OH=-8mA	V_CCO-0.4	—	V
SSTL18_I, V_CCO=1.8×(1±5%) V, V_REF=V_CCO/2, I_OH=-8mA	V_CCO/2+0.47	—	V
SSTL18_II, V_CCO=1.8×(1±5%) V, V_REF=V_CCO/2, I_OH=-13.4mA	V_CCO/2+0.6	—	V
SSTL135, V_CCO=1.35×(1±5%) V, V_REF=V_CCO/2, I_OH=-13mA	V_CCO/2+0.15	—	V

Table 22. IOB differential interface standard output performance (LVDS)

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=2.375V–2.625V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
LVDS					
Output high-level voltage	V_OH	RT=100Ω, connected across Q and QB ports	–	1.675	V
Output low-level voltage	V_OL	RT=100Ω, connected across Q and QB ports	0.825	–	V
Output differential voltage	V_ODIFF	RT=100Ω, connected across Q and QB ports	247	600	mV
Output common-mode voltage	V_OCM	RT=100Ω, connected across Q and QB ports	1.000	1.425	V
Input differential voltage	V_IDIFF	Input common-mode voltage = 1.25V	100	600	mV
Input common-mode voltage	V_ICM	Input differential voltage = ±350 mV	0.300	1.425	V

Table 23. IOB differential interface standard output performance (LVDS_25)

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=2.375V–2.625V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
LVDS_25					
Output high-level voltage	V_OH	RT=100Ω, connected across Q and QB ports	–	1.675	V
Output low-level voltage	V_OL	RT=100Ω, connected across Q and QB ports	0.700	–	V
Output differential voltage	V_ODIFF	RT=100Ω, connected across Q and QB ports	247	600	mV
Output common-mode voltage	V_OCM	RT=100Ω, connected across Q and QB ports	1.000	1.425	V
Input differential voltage	V_IDIFF	—	100	600	mV
Input common-mode voltage	V_ICM	—	0.300	1.5	V

Table 24. SERDES DC characteristics

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCMGTAVCC=0.97V–1.03V, V_CCMGTAVTT=1.17V–1.23V, V_CCO=2.375V–2.625V.

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential peak-to-peak output voltage	DV_PPOUT	TX maximum output swing	1000	—	—	mV
Common-mode output voltage DC (V_CMOUTDC); condition: formula; limit: V_MGTAVTT – D_VPPOUT /4; unit: mV						
Differential output resistance	R_OUT	—	—	100	—	Ω
Output TXP and TXN skew	T_OSKEW	—	—	—	12	ps
Differential peak-to-peak input voltage	DV_PPIN	>10.3125 Gb/s	150	—	1250	mV
Differential peak-to-peak input voltage	DV_PPIN	6.6 Gb/s ~ 10.3125 Gb/s	150	—	1250	mV
Differential peak-to-peak input voltage	DV_PPIN	≤ 6.6 Gb/s	150	—	2000	mV
Differential input resistance	R_IN	—	—	100	—	Ω
Recommended AC coupling capacitor	C_EXT		—	100	—	nf

Table 25. SERDES clock DC characteristics

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCMGTAVCC=0.97V–1.03V, V_CCMGTAVTT=1.17V–1.23V, V_CCO=2.375V–2.625V.

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential peak-to-peak input voltage	V_IDIFF	—	250	—	2000	mV
Differential input resistance	R_IN	—	—	100	—	Ω
Recommended AC coupling capacitor	C_EXT	—	—	100	—	nf

6.2 Switching characteristics

Table 26. Network application interface performance [1]

Characteristic	Symbol	Condition	Limit	Unit
SDR LVDS transmitter rate	DR_SDR_LVDS_TX	Using OSERDES, data width 4 to 8	625	Mb/s
DDR LVDS transmitter rate	DR_DDR_LVDS_TX	Using OSERDES, data width 4 to 14	1250 (HPIO)	Mb/s
DDR LVDS transmitter rate	DR_DDR_LVDS_TX	Using OSERDES, data width 4 to 14	950 (HRIO)	Mb/s
SDR LVDS receiver rate	DR_SDR_LVDS_RX	SPI-4.1(1)	625	Mb/s
DDR LVDS receiver rate	DR_DDR_LVDS_RX	SPI-4.1(1)	1250 (HPIO)	Mb/s
DDR LVDS receiver rate	DR_DDR_LVDS_RX	SPI-4.1(1)	950 (HRIO)	Mb/s

Note 1: The performance achieved by the LVDS receiver must rely on a specific dynamic phase-alignment (DPA) algorithm.

Table 27. Maximum physical interface (PHY) rate for memory interface IP available in the memory interface generator [1,2]

Characteristic	Symbol	Condition	Limit	Unit
4:1 memory control				
DDR3	PHYR_DDR3_4	V_CCAUX_IO=2.0V	1600 (HPIO)	Mb/s
DDR3	PHYR_DDR3_4	V_CCAUX_IO=1.8V	1066 (HPIO)	Mb/s
DDR3	PHYR_DDR3_4	-	800 (HRIO)	Mb/s
DDR3L	PHYR_DDR3L_4	V_CCAUX_IO=2.0V	1333 (HPIO)	Mb/s
DDR3L	PHYR_DDR3L_4	V_CCAUX_IO=1.8V	800 (HPIO)	Mb/s
DDR3L	PHYR_DDR3L_4	-	667 (HRIO)	Mb/s
DDR2	PHYR_DDR2_4	V_CCAUX_IO=2.0V	800 (HPIO)	Mb/s
DDR2	PHYR_DDR2_4	V_CCAUX_IO=1.8V	800 (HPIO)	Mb/s
DDR2	PHYR_DDR2_4	-	800 (HRIO)	Mb/s
RLDRAM III	PHYR_RLDRAMIII_4	V_CCAUX_IO=2.0V	667 (HPIO)	Mb/s
RLDRAM III	PHYR_RLDRAMIII_4	V_CCAUX_IO=1.8V	450 (HPIO)	Mb/s
2:1 memory control				
DDR3	PHYR_DDR3_2	V_CCAUX_IO=2.0V	800 (HPIO)	Mb/s
DDR3	PHYR_DDR3_2	V_CCAUX_IO=1.8V	800 (HPIO)	Mb/s

Table 27. Maximum physical interface (PHY) rate for memory interface IP available in the memory interface generator [1,2] (continued)

Characteristic	Symbol	Condition	Limit	Unit
2:1 memory control (continued)				
DDR3	PHYR_DDR3_2	-	800 (HRIO)	Mb/s
DDR3L	PHYR_DDR3L_2	V_CCAUX_IO=2.0V	800 (HPIO)	Mb/s
DDR3L	PHYR_DDR3L_2	V_CCAUX_IO=1.8V	800 (HPIO)	Mb/s
DDR3L	PHYR_DDR3L_2	-	667 (HRIO)	Mb/s
DDR2	PHYR_DDR2_2	V_CCAUX_IO=2.0V	800 (HPIO)	Mb/s
DDR2	PHYR_DDR2_2	V_CCAUX_IO=1.8V	800 (HPIO)	Mb/s
DDR2	PHYR_DDR2_2	-	800 (HRIO)	Mb/s
QDR II+(2)	PHYR_QDRIIP_2	V_CCAUX_IO=2.0V	450 (HPIO)	Mb/s
QDR II+(2)	PHYR_QDRIIP_2	V_CCAUX_IO=1.8V	450 (HPIO)	Mb/s
QDR II+(2)	PHYR_QDRIIP_2	-	400 (HRIO)	Mb/s
RLDRAM II	PHYR_RLDRAMII_2	V_CCAUX_IO=2.0V	450 (HPIO)	Mb/s
RLDRAM II	PHYR_RLDRAMII_2	V_CCAUX_IO=1.8V	450 (HPIO)	Mb/s
RLDRAM II	PHYR_RLDRAMII_2	-	450 (HRIO)	Mb/s
LPDDR2	PHYR_LPDDR2_2	V_CCAUX_IO=2.0V	667 (HPIO)	Mb/s
LPDDR2	PHYR_LPDDR2_2	V_CCAUX_IO=1.8V	667 (HPIO)	Mb/s
LPDDR2	PHYR_LPDDR2_2	-	667 (HRIO)	Mb/s

Note 1: When internal V_REF is used, the maximum data rate is 800Mb/s (400MHz).

Note 2: The QDR II+ maximum performance specification applies to implementations with a burst length of 4 (BL=4).

Table 28. Clock buffer and network frequency characteristics

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Maximum global clock tree frequency	f_MAX_BUFG	-	—	464.00	MHz
Maximum I/O clock tree frequency	f_MAX_BUFIO	-	—	600.00	MHz
Maximum regional clock tree frequency	f_MAX_BUFR	-	—	315.00	MHz
Maximum horizontal clock buffer frequency	f_MAX_BUFH	-	—	464.00	MHz

Table 29. MMCM module switching characteristics

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Minimum clock input frequency	MMCM_f_INMIN	-	10	—	MHz
Maximum clock input frequency	MMCM_f_INMAX	-	—	800	MHz
Minimum MMCM VCO frequency	MMCM_f_VCOMIN	-	600	—	MHz
Maximum MMCM VCO frequency	MMCM_f_VCOMAX	-	—	1200	MHz

Table 29. MMCM module switching characteristics (continued)

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Minimum output frequency	MMCM_f_OUTMIN	-	4.69	—	MHz
Maximum output frequency	MMCM_f_OUTMAX	-	—	800	MHz
Minimum phase detector frequency	MMCM_f_PFDMIN	-	10	—	MHz
Maximum phase detector frequency	MMCM_f_PFDMAX		—	450	MHz

Table 30. PLL module switching characteristics

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.14V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Minimum clock input frequency	PLL_f_INMIN	-	19	—	MHz
Maximum clock input frequency	PLL_f_INMAX	-	—	800	MHz
Minimum PLL VCO frequency	PLL_f_VCOMIN	-	800	—	MHz
Maximum PLL VCO frequency	PLL_f_VCOMAX	-	—	1600	MHz
Minimum output frequency	PLL_f_OUTMIN	-	6.25	—	MHz
Maximum output frequency	PLL_f_OUTMAX	-	—	800	MHz
Minimum phase detector frequency	PLL_f_PFDMIN	-	19	—	MHz
Maximum phase detector frequency	PLL_f_PFDMAX	-	—	450	MHz

Table 31. Pin-to-pin input and output parameters

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.425V–1.575V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Delay from clock input pin to output flip-flop output pin (closest to BUFGs)	t_ICKOF	SSTL15, Fast Slew Rate, without MMCM and PLL	—	7.08	ns
Delay from clock input pin to output flip-flop output pin (farthest from BUFGs)	t_ICKOFFAR	SSTL15, Fast Slew Rate, without MMCM and PL	—	7.40	ns
Delay from clock input pin to output flip-flop output pin (using MMCM)	t_ICKOFMMCMCC	SSTL15, Fast Slew Rate, using MMCM	—	1.03	ns
Delay from clock input pin to output flip-flop output pin (using PLL)	t_ICKOFPLLCC	SSTL15, Fast Slew Rate, using PLL	—	0.82	ns

Table 32. eFUSE programming characteristics [1]

Characteristic	Symbol	Condition	Min.	Max.	Unit
Programming temperature range	T_J		15	125	°C
V_CCAUX programming current	I_FS		—	115	mA

Note: (1) The PL device must be prevented from being configured during eFUSE programming.

Table 33. GTX transceiver frequency characteristics

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCAUX_IO=1.71V–1.89V, V_MGTAVCC=0.97V–1.08V, V_MGTAVTT=1.17V–1.23V, V_MGTVCCAUX=1.75V–1.85V, V_CCO=1.14V–3.465V (HRIO) or V_CCO=1.14V–1.89V (HPIO).

Characteristic	Symbol	Condition	Min.	Max.	Unit
GTX transceiver maximum data rate	f_GTXMAX		12.5	—	Gb/s
GTX transceiver minimum data rate	f_GTXMIN		—	0.500	Gb/s

Table 34. CPU clock switching characteristics

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Maximum CPU clock frequency	f_CPU_6X4X_621_MAX	Clock ratio set to 6:2:1	—	766	MHz
Maximum CPU_3X clock frequency	f_CPU_3X2X_621_MAX	Clock ratio set to 6:2:1	—	383	MHz
Maximum CPU_2X clock frequency	f_CPU_2X_621_MAX	Clock ratio set to 6:2:1	—	255	MHz
Maximum CPU_1X clock frequency	f_CPU_1X_621_MAX	Clock ratio set to 6:2:1	—	127	MHz
Maximum CPU clock frequency	f_CPU_6X4X_421_MAX	Clock ratio set to 4:2:1	—	600	MHz
Maximum CPU_3X clock frequency	f_CPU_3X2X_421_MAX	Clock ratio set to 4:2:1	—	300	MHz
Maximum CPU_2X clock frequency	f_CPU_2X_421_MAX	Clock ratio set to 4:2:1	—	300	MHz
Maximum CPU_1X clock frequency	f_CPU_1X_421_MAX	Clock ratio set to 4:2:1	—	150	MHz

Table 35. DDR clock switching characteristics

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Maximum DDR3 interface performance	f_DDR3_MAX	—	—	1066	Mb/s

Table 36. PS-PL interface switching characteristics

Unless otherwise specified: V_CCINT=0.97V–1.03V, V_CCBRAM=0.97V–1.03V, V_CCAUX=1.71V–1.89V, V_CCO=1.425V–1.575V, V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Maximum AXI interface performance	f_AXI_MAX	—	—	250	MHz

Table 37. PS-PLL interface switching characteristics

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
PLL maximum output frequency	f_PSPLL_MAX	—	—	1600	MHz

Table 38. Processor configuration access port switching characteristics

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Processor configuration access port maximum frequency	f_PCAPCK	—	—	100	MHz

Table 39. SPI master mode interface switching characteristics

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
SPI master mode device clock frequency	f_MSPICLK	—	—	50	MHz
SPI reference clock frequency	f_SPI_REF_CLK	—	—	200	MHz

Table 40. SPI slave mode interface switching characteristics

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
SPI slave mode device clock frequency	f_SSPICLK	—	—	25	MHz
SPI reference clock frequency	f_SPI_REF_CLK	—	—	200	MHz

Table 41. UART interface switching characteristics

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Maximum transmit baud rate	B_AUDTXMAX	—	—	1	Mb/s
Maximum receive baud rate	B_AUDRXMAX	—	—	1	Mb/s
UART reference clock frequency	f_UART_REF_CLK		—	100	MHz

Table 42. Watchdog timer switching characteristics

Unless otherwise specified: V_CCPINT=0.97V–1.03V, V_CCPAUX=1.71V–1.89V, V_CCPLL=1.71V–1.89V, V_CCO_DDR=1.14V–1.89V, V_CCO_MIO=1.71V–3.465V.

Characteristic	Symbol	Condition	Min.	Max.	Unit
Watchdog timer input clock frequency	f_WDTCLK	—	—	10	MHz

7. Functional description

7.1 Overview

The processing system of EKT7Z045 includes an ARM dual-core Cortex-A9 hard-core processor, with a single-/double-precision floating-point NEON unit in each processor; each processor has its own 32KB instruction cache and 32KB data cache (L1 cache); 512KB of L2 cache; 256KB of on-chip memory; support for DDR3 external memory; support for external static memories such as QSPI, NAND and NOR; 8 DMA channels; 2 UARTs, 2 CANs, 2 I2Cs, 2 SPIs, 4 32-bit GPIOs, 2 USB2.0 interfaces, 2 tri-speed Ethernet interfaces, 2 SD/SDIO interfaces, and support for AXI interfaces. At the same time, the programmable logic of the EKT7Z045 series

circuits has abundant resources, including 85K programmable logic cells, 220 DSPs, 4.9Mb of programmable Block RAM, 106400 flip-flops, and 53200 look-up tables (LUTs).

7.2 Functional description

7.2.1 Processing system functional description

7.2.1.1 Application processing unit APU

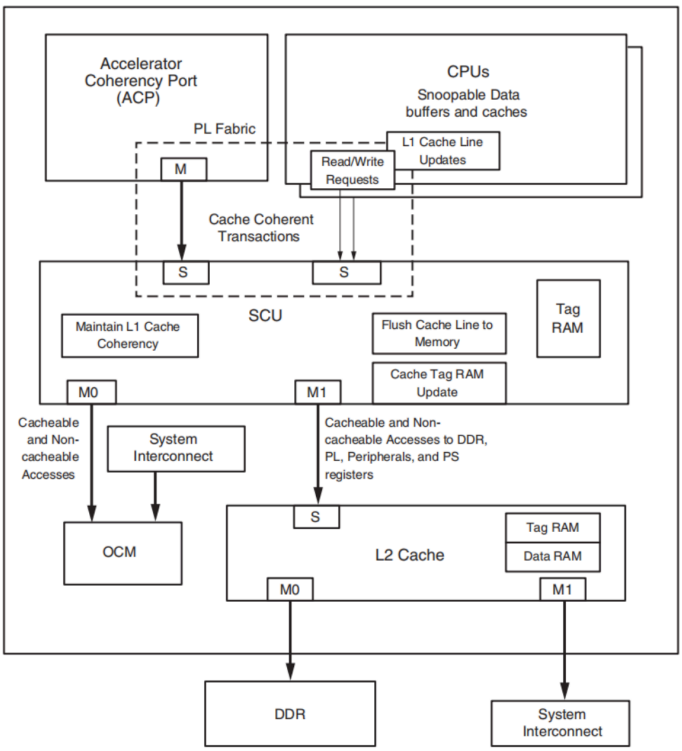


Figure 6. APU structural block diagram

The APU block diagram is shown above. It consists mainly of two ARM Cortex-A9 MPCore processors. Each ARM core includes a SIMD media processing engine (NEON), a memory management unit (MMU), and a level-1 cache (divided into instruction L1 (I) and data L1 (D) sections). The APU includes a level-2 cache and an on-chip memory (OCM). It also includes an accelerator coherency port (ACP) to facilitate communication between the PL and APU. The PL can access the level-2 cache/OCM through a 64-bit AXI interface while maintaining CPU L1 cache memory coherency. Finally, a snoop control unit (SCU) forms a bridge between the ARM cores and the level-2 cache/OCM; this unit is also responsible for interfacing with the PL, as shown above. The functions of the modules are described below:

MMU: The main task of the MMU is to translate virtual addresses into physical addresses;

Cache: The level-1 and level-2 caches store instructions and data;

SCU: The SCU performs interface tasks between the two processors and the level-1 and level-2 caches;

NEON: As an additional function of the ARM processor, the NEON engine implements single-instruction multiple-data (SIMD) functionality to accelerate media and DSP algorithms. NEON can perform the same operation simultaneously on multiple sets of data in the input vector to obtain the corresponding output vector. This type of computation is mainly used in image and video processing,

where large numbers of data samples (pixels) can be processed simultaneously. It is also suitable for common signal-processing functions with parallelism, such as finite impulse response (FIR) filtering and fast Fourier transform (FFT). It should be noted that NEON supports multiple data types, including signed and unsigned integers, single-precision floating-point numbers and half-precision floating-point numbers, but does not support double precision.

FPU: This unit implements IEEE 754-compatible hardware acceleration of floating-point arithmetic, supports single- and double-precision formats, and also partially supports half-precision and integer conversion.

7.2.1.2 DMA

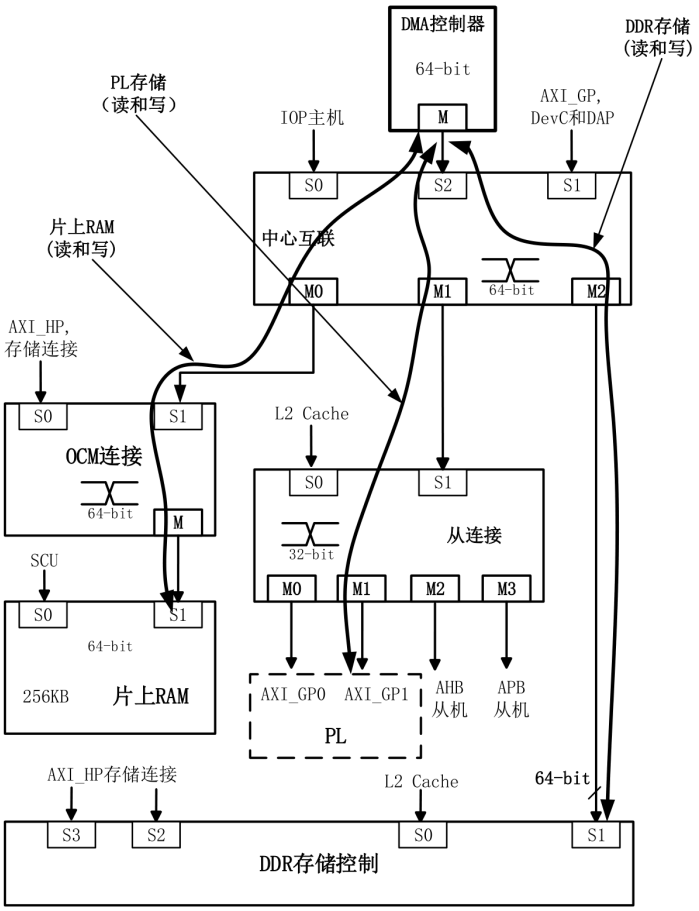


Figure 7. DMA structural block diagram

Diagram labels: DMA controller; DDR memory (read and write); PL memory (read and write); IOP master; central interconnect; on-chip RAM (read and write); AXI_HP memory link; OCM link; slave interconnect; on-chip RAM; AHB slave; APB slave; DDR memory controller.

The DMA controller (DMAC) uses a 64-bit AXI master interface running at twice the CPU clock rate to perform DMA data transfers to and from system memory and PL peripherals. The DMAC mainly includes three submodules: the interface module for memory/peripherals, the DMA instruction execution engine, and the MFIFO data buffer module. The DMAC also includes two sets of control/status registers for the three main functional modules, which can be accessed in secure or non-secure mode, respectively.

7.2.1.3 External memory interface DDR

The DDR memory controller supports DDR2, DDR3 and DDR3L devices. It consists of three main modules: the AXI memory port interface (DDRI), the core controller with a transaction scheduler (DDRC), and the controller with a digital PHY (DDRP).

The DDRI module is connected to four 64-bit synchronous AXI interfaces and serves multiple AXI masters at the same time. Each AXI interface has its own dedicated transaction FIFO.

DDRC contains two 32-entry content-addressable memories (CAM) for DDR data-transfer scheduling to maximize DDR memory efficiency. It also includes a fly-by path for low-latency channels that can access DDR memory without passing through CAM.

The PHY processes read/write requests from the controller and translates them into specific signals within the timing constraints of the target DDR memory. Signals from the controller are used by the PHY to generate internal signals, which are connected to pins through the digital PHY. The DDR pins connect directly to the DDR device via PCB signal traces.

The system accesses DDR through the four 64-bit synchronous AXI memory ports of the DDRI. One AXI port is dedicated to the L2-cache of the CPU and ACP, two ports are dedicated to the AXI_HP interfaces, and the fourth port is shared by all other masters on the AXI interconnect.

The DDR interface (DDRI) arbitrates requests from 8 ports (4 reads and 4 writes). The arbiter selects requests and passes them to the DDR controller and transaction scheduler (DDRC). Arbitration is based on a combination of the time the request has been waiting, its urgency, and whether the request is within the same page as the preceding request.

The DDRC receives requests from DDRI through a single interface. Reads and writes both pass through this interface. A read request contains a tag field, which is returned together with the DDR data. The DDR controller PHY (DDRP) drives DDR transactions.

7.2.1.4 MIO/EMIO

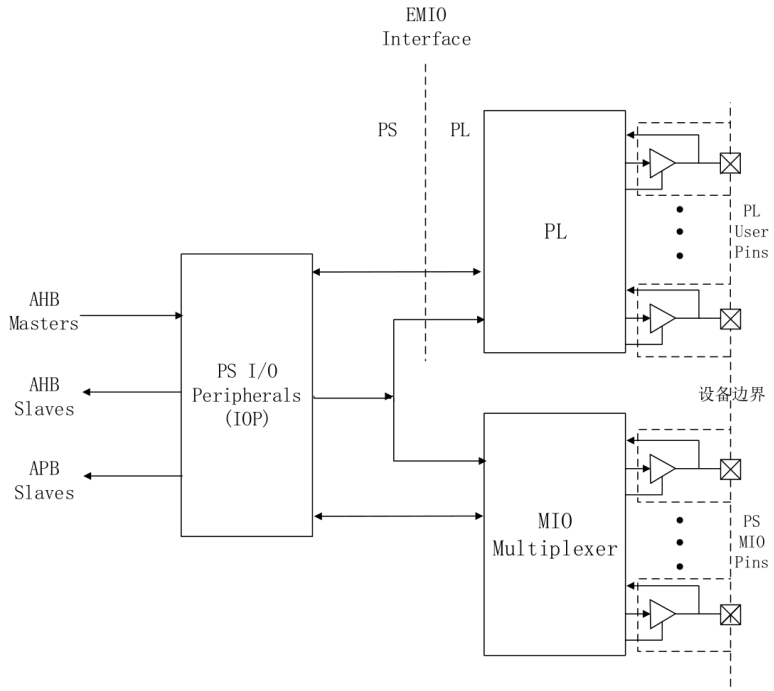


Figure 8. MIO structural block diagram

Diagram label: Device boundary.

Because the number of MIO pins is limited, MIO multiplexing is necessary for connecting I/O peripherals. Routing of I/O signals to MIO pins is software-programmable. I/O peripheral signals can also be routed into PL devices via the EMIO interface, and routed to PL device pins when necessary. Routing I/O signals to EMIO makes effective use of PL pins to obtain more device pins; at the same time it permits I/O peripheral controllers to connect to user logic in the PL.

7.2.1.5 SD

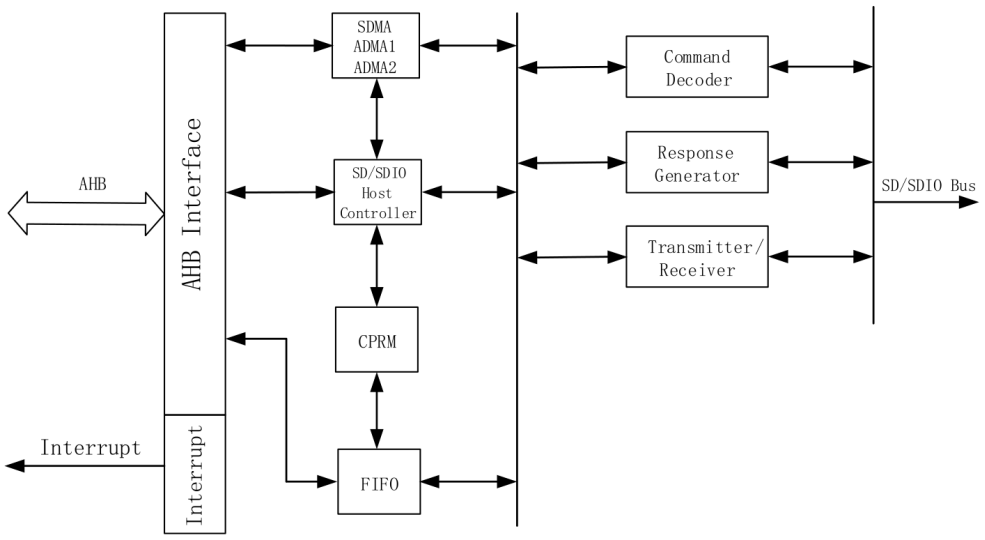


Figure 9. SD structural block diagram

The SD/SDIO controller communicates with SDIO devices and SD memory cards through up to 4 data lines. On the SD interface, one data line or four data lines can be used for data transmission. The SDIO interface can be routed to MIO pins through the MIO multiplexer, or through EMIO to SelectIO pins in the PL.

7.2.1.6 XADC

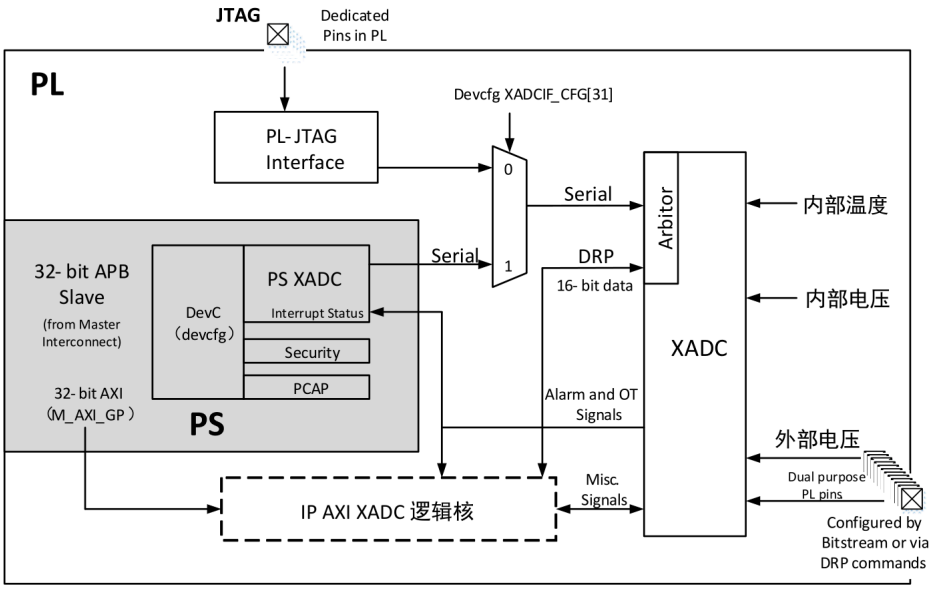


Figure 10. XADC structural block diagram

Diagram labels: Internal temperature; internal voltage; external voltage; IP AXI XADC logic core.

The XADC has two 12-bit 1 million samples per second (MSPS) ADCs, with independent track-and-hold amplifiers, an analog multiplexer (up to 17 external analog input channels), and on-chip thermal and voltage sensors. These two ADCs can be configured to sample two external analog input channels simultaneously. The sample-and-hold amplifiers support a range of analog input signal types, including unipolar, bipolar and differential. The analog inputs can support a signal bandwidth of 500KHz at a sampling rate of 1MSPS. An external analog multiplexer can be used to increase the number of supported external channels without requiring additional package pins.

The XADC can optionally use the on-chip reference circuit to achieve basic on-chip monitoring of temperature and power rails without external active components. To achieve the full 12-bit performance of the ADC, an external 1.25V reference IC is recommended.

The most recent measurement results (together with the maximum and minimum readings) are stored in dedicated registers. User-defined alarm thresholds can automatically indicate overtemperature events and unacceptable supply variations. A user-specified limit (for example, 100°C) can be used to initiate a software-controlled system power-off.

7.2.1.7 Tri-speed Ethernet

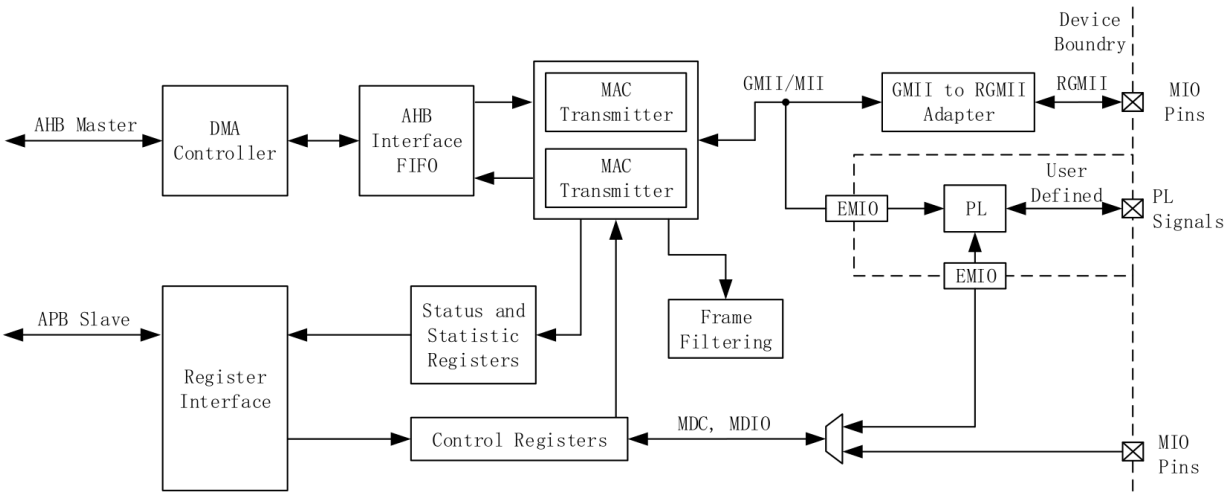


Figure 11. Tri-speed Ethernet structural block diagram

The Gigabit Ethernet controller implements a 10/100/1000Mb/s Ethernet MAC compatible with IEEE802.3-2008, and can operate in half-duplex or full-duplex mode at all three rates. The PS is equipped with two Gigabit Ethernet controllers. Each controller can be configured independently. When accessing pins through MIO, an RGMII interface can be used to save pins. When accessing PL through EMIO, EMIO provides a GMII interface.

The GMII interface available in EMIO can be used to create other Ethernet communication interfaces in the PL.

Registers are used to configure MAC functions, select different operating modes, and enable and monitor network-management statistics. The DMA controller is connected to memory using the AHB bus interface. The DMA controller is connected to the FIFO interface of the MAC controller, providing scatter-gather capability for storing embedded processing system data packets.

7.2.1.8 UART

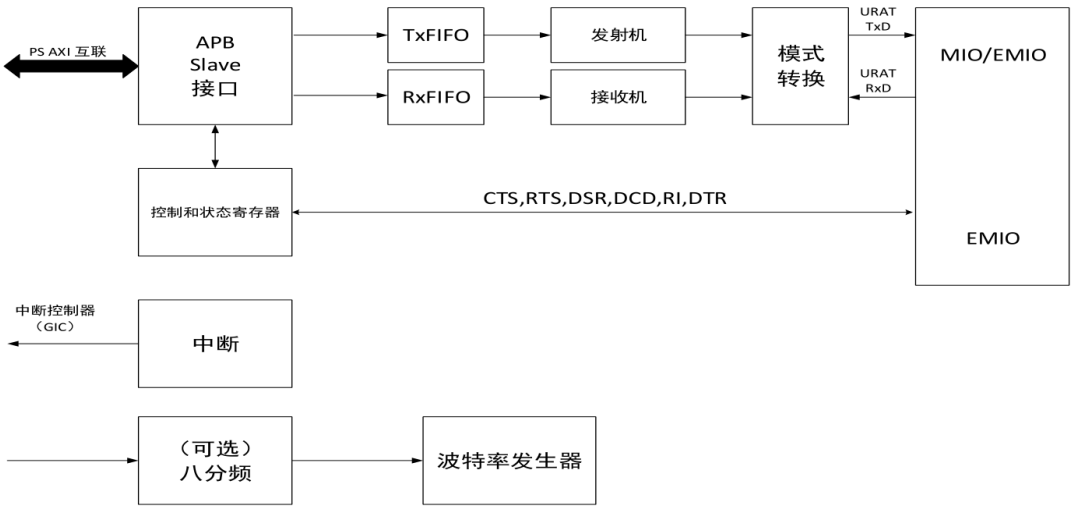


Figure 12. UART structural block diagram

Diagram labels: PS AXI interconnect; APB slave interface; transmitter; receiver; mode conversion; control and status registers; interrupt controller (GIC); interrupt; divide by eight (optional); baud-rate generator.

The UART controller is a full-duplex asynchronous receiver and transmitter supporting a wide range of programmable baud rates and I/O signal formats. It can accommodate automatic parity generation and multi-master detection modes.

UART operation is controlled by configuration and mode registers. The status, interrupt status and modem status registers are used to read the status of FIFOs, modem signals and other controller functions.

The controller consists of separate Rx and Tx data paths. Each path includes a 64-byte FIFO. The controller serializes and deserializes data in the Tx and RxFIFOs and includes a mode switch to support various loopback configurations of RxD and TxD signals. FIFO interrupt status bits support polling or interrupt-driven handlers. Software reads and writes data bytes through the Rx and Tx data port registers.

When UART is used for modem applications, the modem control module detects and generates modem handshake signals and controls the receiver and transmitter paths according to the handshake protocol.

7.2.1.9 I2C

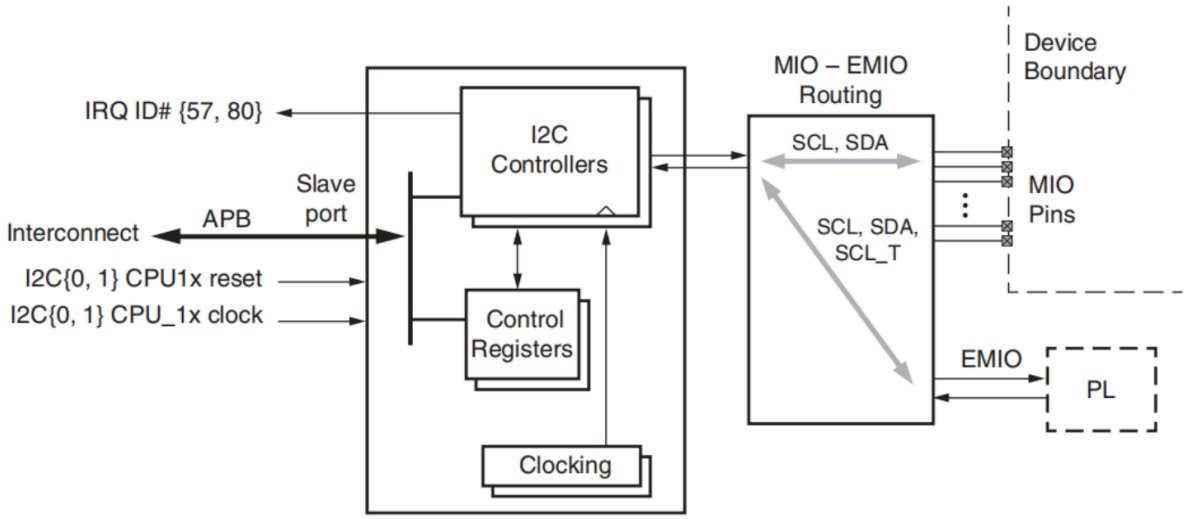


Figure 13. I2C structural block diagram

This I2C module is a bus controller that can operate as master or slave in a multi-master design and supports a wide clock frequency range from DC to 400kb/s.

In master mode, a transfer can only be initiated by the processor writing the slave address into the I2C address register; the processor is notified of any available received data by a data interrupt or transfer-complete interrupt. If the HOLD bit is set, the I2C interface holds the SCL line low after completing data transfer, supporting low-speed processor service and preventing slave overflow. Master mode supports 7-bit address (normal) mode and 10-bit address (extended) mode.

In slave monitor mode, the I2C interface is set as a master while attempting to transfer data to a specific slave until the slave responds with ACK. The HOLD bit can also be set to prevent the master from continuing the transfer and avoid slave overflow.

A common feature of master and slave modes is the (TO) interrupt flag. If at any time the master or addressed slave holds the SCL line low longer than the time specified by the timeout register, a TO interrupt is generated to prevent a stall.

7.2.1.10 SPI

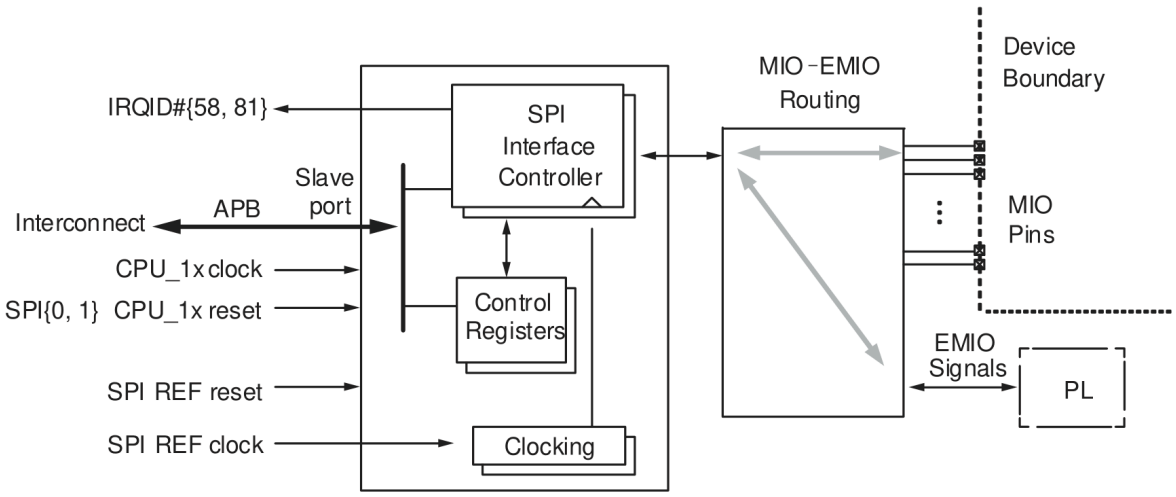


Figure 14. SPI structural block diagram

The SPI bus controller supports communication with various peripherals, such as memory, temperature sensors, analog converters, real-time clocks, displays and any SD card supporting serial mode. The SPI controller can operate in master, slave or multi-master mode. It includes two SPI controllers based on the Cadence SPI core.

In master mode, the controller drives the serial clock, and slave selection supports SPI multi-master mode. The serial clock originates from the PS clock subsystem. The controller uses up to 3 separate slave select (SS) output signals to initiate messages; these signals can be expanded externally. The controller reads and writes slave devices by writing data to a 32-bit read/write data port register.

In multi-master mode, the controller tri-states its output signals when not active and can detect contention errors when enabled. When the SPI enable bit is reset, the output signals are immediately tri-stated and the interrupt status register indicates the mode fault.

In slave mode, the controller receives the serial clock from an external device and uses SPI_Ref_Clk to synchronize data acquisition. Slave mode includes a programmable start-detection mechanism to enable normal operation when the controller is enabled and SS is asserted.

Read and write FIFOs provide buffering between the SPI I/O interface and software servicing the controller through the APB slave interface. The FIFOs are used in slave and master I/O modes.

7.2.1.11 GPIO

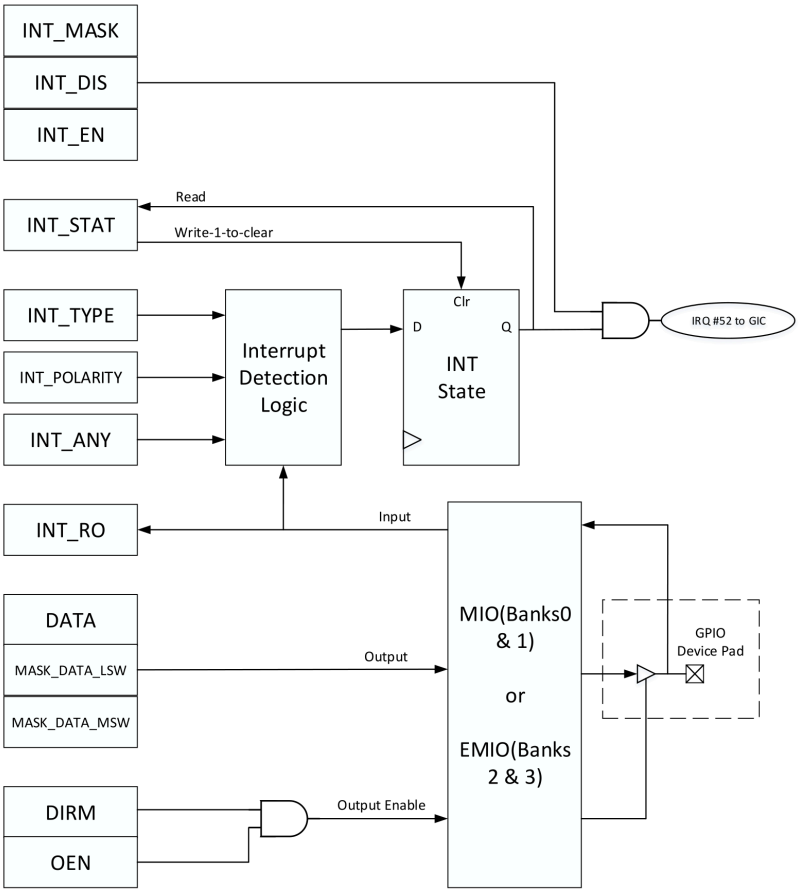


Figure 15. GPIO structural block diagram

The general-purpose I/O (GPIO) peripheral provides software observation and control of up to 54 device pins through the MIO module. It also provides access to 64 inputs from the programmable logic (PL) and access to 128 PL outputs through the EMIO interface. GPIO is organized into four register banks, and related interface signals are grouped.

Each GPIO is independently and dynamically programmed as input, output or interrupt response. Software can use a single load instruction to read all GPIO values in the bank, or use a single store instruction to write data to one or more GPIOs (within the GPIO range). GPIO control and status registers are mapped to memory at base address 0xE000_A000.

7.2.1.12 USB

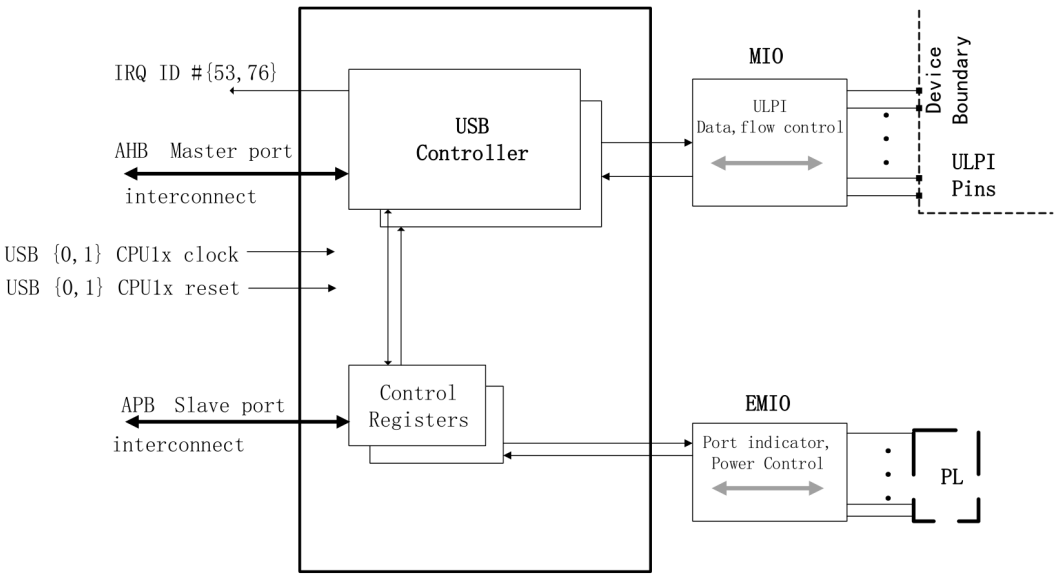


Figure 16. USB structural block diagram

Two independent USB controllers have separate control and status registers. Each ULPI interface is independently enabled through MIO, and each controller routed through EMIO has its own port indicator and power signals.

7.2.2 Programmable logic functional description

The PL side mainly consists of resources such as configurable logic blocks (CLB), input/output blocks (IOB), 36Kbit capacity memory blocks (BRAM), digital signal processing blocks (DSP), digital clock management blocks (CMT), and interconnect routing blocks.

CLB functions include: look-up tables; global carry chain; two adder carry chains; D flip-flop (DFF) function (synchronous/asynchronous, SR high/low); LATCH function; CLB internal carry-chain exclusive OR gate XOR, carry selector MUXCY; CLB internal carry-chain AND gate MULT_AND; multiplexer MUXF5 and MUXF6 functions; shift-register function; distributed RAM function.

IOB functions: IOBUF, ILOGIC, OLOGIC, supporting LVDS rates of 1.25Gbps.

BRAM function: internal 36Kbit memory unit supporting access in dual-port (A, B ports) or single-port RAM mode.

DSP function: supports multiple independent function operations, including multiplication, multiply-accumulate (MACC), multiply-add, three-input addition, comparators and wide-range counters.

CMT: frequency division/multiplication/mixing/phase shifting/locking, etc.

7.2.2.1 High-performance IO module

The high-performance IO module consists of the IO input/output block (IOB), IDELAYE, ODELAYE, and corresponding ILOGICE/ISERDESE and OLOGICE/OSERDESE. It is suitable for IO with high-performance requirements, such as high-speed memory interfaces or chip-to-chip connections with voltages up to 1.8V.

Table 43. Levels and features supported by high-performance IO Bank

No.	Characteristic	High-performance IO Bank
1	3.3V IO	NA
2	2.5V IO	NA
3	1.8V IO	Supported
4	1.5V IO	Supported
5	1.35V IO	Supported
6	1.2V IO	Supported
7	LVDS level	Supported
8	24mA LVCMOS18, LVTTL output	NA
9	V_CCAUX_IO supply	Supported
10	Digitally controlled impedance (DCI) and DCI cascading	Supported
11	Internal V_REF	Supported
12	Internal differential termination (DIFF_TERM)	Supported
13	IDELAY	Supported
14	ODELAY	Supported
15	IDELAYCTRL	Supported
16	ISERDES	Supported
17	OSERDES	Supported
18	ZHOLD_DELAY	NA

Table 44. High-performance IO module functions

No.	Internal module function
1	Tri-state
2	Edge-triggered D flip-flop input/output function
3	Level-sensitive latch input/output function
4	IDDR function in different modes (OPPOSITE_EDGE/SAME_EDGE/SAME_EDGE_PIPELINED)
5	ODDR function in different modes (SAME_EDGE, OPPOSITE_EDGE)
6	Input serial-to-parallel conversion function
7	Output parallel-to-serial conversion function
8	IDELAY/ODELAY function
9	IO_FIFO function (4x4, 4x8/8x4, cascade)

7.2.2.2 Wide-range IO module

The wide-range IO (HRIO) module consists of the IO input/output block (IOB), IDELAY, and corresponding ILOGICE/ISERDESE and OLOGICE/OSERDESE. It is suitable for IO with wide-range requirements, such as high-speed memory interfaces or chip-to-chip connections with voltages up to 3.3V.

Table 45. Levels and features supported by wide-range IO Bank

Characteristic	Wide-range IO Bank
3.3V IO	Supported
2.5V IO	Supported
1.8V IO	Supported
1.5V IO	Supported
1.35V IO	Supported
1.2V IO	Supported
LVDS level	Supported
24mA LVCMOS18, LVTTL output	Supported
V_CCAUX_IO supply	NA
Digitally controlled impedance (DCI) and DCI cascading	NA
Internal V_REF	Supported
Internal differential termination (DIFF_TERM)	Supported
IDELAY	Supported
ODELAY	NA
IDELAYCTRL	Supported
ISERDES	Supported
OSERDES	Supported
ZHOLD_DELAY	NA

Table 46. Wide-range IO module functions

No.	Internal module function
1	Tri-state
2	Edge-triggered D flip-flop input/output function
3	Level-sensitive latch input/output function
4	IDDR function in different modes (OPPOSITE_EDGE/SAME_EDGE/SAME_EDGE_PIPELINED)
5	ODDR function in different modes (SAME_EDGE, OPPOSITE_EDGE)
6	Input serial-to-parallel conversion function
7	Output parallel-to-serial conversion function
8	IDELAY function
9	IO_FIFO function (4x4, 4x8/8x4, cascade)

7.2.2.3 CLB module

Configurable logic blocks (CLBs) are the main modules for implementing user-defined sequential and combinational logic functions. Configurable logic units can be interconnected through interconnect matrices and connected to other product resources through interconnect arrays. The complexity and quantity of configurable logic units are important parameters of product programmability.

The main features of the CLB module are:

• True 6-input look-up table (LUT)

• Dual LUT5 (5-input LUT) operation

• Distributed memory and shift-register logic

• Dedicated carry logic for arithmetic functions

• Wide multiplexers for efficient use

Each LUT can be configured as a LUT with 6 inputs and 1 output, or as two LUTs with 5 inputs and 2 independent outputs, using common address or input logic. Each LUT output can optionally be registered. One CLB unit contains four 6-input LUTs and eight associated flip-flops, multiplexers and arithmetic carry logic. Two CLB units form one CLB module. Four flip-flops in each CLB unit (one flip-flop per LUT) can be configured for latch operation; the remaining four flip-flops must remain unused.

Approximately 1/3 of the CLB units are SLICEL logic and the remaining units are SLICEM logic. SLICEM logic can use its LUTs as distributed 64bit RAM, or as a 32bit shift register (SRL32) or two SRL16s.

7.2.2.4 BRAM module

The BRAM module, or Block RAM module, can store 36K bit of data or be divided into two independent 18K bit memory modules. The Block RAM module can be configured as RAM and FIFO in various modes.

The main features of the Block RAM module include:

• Each BRAM can store up to 36Kbit of data

• Each BRAM supports two independent 18Kb blocks or a single 36Kb block

• Each 36Kb BRAM can be set to simple dual-port mode, with double data width supporting 72bit. An 18Kb BRAM can be set to simple dual-port mode with double data width supporting 36bit. Simple dual-port mode is defined as one read-only and one write-only port with independent clocks.

• Simple dual-port mode supports a fixed width at one port and a variable width at the other.

• Adjacent BRAMs can be combined into a 64K×1 memory without additional logic.

• 64bit ECC supports each 36Kb BRAM or 36Kb FIFO, with separate encoding and decoding functions. ECC mode supports error injection.

• The BRAM output latch and register modes can be synchronously set/reset to initial values.

• BRAM can be configured as a synchronous FIFO to eliminate uncertain flag bits.

• FULL flag.

• 18-, 36- and 72bit BRAM ports can be written independently by byte. This function is often used for microprocessor interfaces.

• Each BRAM includes an operating address sequence and control circuitry to generate a built-in dual-clock FIFO memory; BRAM can be set to an 18 Kb or 36 Kb FIFO.

• All inputs are registered via the port clock and have clock setup timing specifications.

• All outputs have a read function or a read-during-write function determined by the write-enable (WE) pin. Outputs become available after the clock-to-output interval. Read-during-write outputs can select one of three operating modes: WRITE_FIRST, READ_FIRST and NO_CHANGE.

• Write operations require one clock edge.

• Read operations require one clock edge.

• All output ports are latched or registered. The output port state does not change before another read/write operation. BRAM defaults to latch mode.

• Output data depth can be operated through internal pipeline registers. Register mode is strongly recommended, as it permits a higher clock frequency while adding one clock cycle of latency.

BRAM usage rules include:

• The synchronous set and reset (RSTRAM) port cannot be used while the ECC decoder is in use (EN_ECC_READ=TRUE).

• The BRAM synchronous output register (optional), when DO_REG=1, is set or reset (SRVAL) through RSTREG. When RSTREG takes priority over REGCE, RSTREG_PRIORITY determines the priority. When DO_REG=0 or 1, the synchronous output latch is set or reset (SRVAL) by RSTRAM.

• Setup times for BRAM address or write-enable pins must not be violated. Violation of address setup time causes loss of BRAM data contents.

• If RSTREG_PRIORITY is set to REGCE, BRAM register-mode RSTREG requires REGCE=1 to reset the output DO register value. BRAM array data output latches cannot be reset through this mode. BRAM latch-mode RSTRAM requires BRAM enable EN=1 to reset the output DO latch value.

• Two BRAM primitives, RAMB36E1 and RAMB18E1. The RAM_MODE attribute defines the BRAM mode as either SDP mode or true dual-port (TDP) mode.

• When using special BRAM primitives, different read/write port widths can be selected. Parity bits are used only for x9, x18 and x36 port widths. Parity bits cannot be used for x1, x2 and x4 read widths. If the read width is x1,x2,x4, the effective write width is x1,x2,x4,x8,x16,x32. Similarly, if the write width is x1,x2,x4, the actual effective read width is x1,x2,x4,x8,x16,x32, depending on the primitive attributes respectively set to 1,2,4,9,18,36.

Table 47. Main BRAM module functions

No.	Internal module function
1	BRAM read/write functions in different modes (WRITE_FIRST, READ_FIRST, NO_CHANGE)
2	BRAM read/write function at different widths and depths (SDP, TDP): 36Kbit RAM: 64Kx1, 32Kx1, 16Kx2, 8Kx4, 4Kx9, 2Kx18, 1Kx36, 512x72 18Kbit RAM: 16Kx1, 8Kx2, 4Kx4, 2Kx9, 1Kx18, 512x36
3	RAM output register (RSTREG, DO_REG)
4	Independent read/write width function
5	BRAM cascade function
6	FIFO functions in different modes and status flag testing (synchronous or asynchronous, standard or first-word fall-through, FWFT)
7	FIFO output register testing
8	FIFO functions at different depths and widths: 18Kb: 4K x 4, 2K x 9, 1K x 18, 512 x 36 36Kb: 8K x 4, 4K x 9, 2K x 18, 1K x 36, 512 x 72
9	FIFO36 cascade and parallel functions; BRAM and FIFO combination connection function
10	64 bit ECC functions in different modes (Standard, encode only, decode only)
11	RAM ECC, FIFO ECC function
12	ECC output register function

Table 48. BRAM module application scenarios

Primitive	Set read width	Set write width	Effective read width	Effective write width
RAMB18E1	1, 2, 4	9,18	Same as set	8,16
RAMB18E1	9,18	1, 2, 4	8,16	Same as set
RAMB18E1	1, 2, 4	1, 2, 4	Same as set	Same as set
RAMB18E1	9,18	9,18	Same as set	Same as set
RAMB36E1	1, 2, 4	9,18,36	Same as set	8,16,32
RAMB36E1	9,18,36	1, 2, 4	8,16,32	Same as set
RAMB36E1	1, 2, 4	1, 2, 4	Same as set	Same as set

Table 48. BRAM module application scenarios (continued)

Primitive	Set read width	Set write width	Effective read width	Effective write width
RAMB36E1	9,18,36	9,18,36	Same as set	Same as set

7.2.2.5 DSP module

DSP supports multiple functions, including multiplication, multiply-accumulate (MACC), multiply-add, three-input addition, barrel shifting, wide bus selection, numerical comparison, bitwise logic operations, pattern detection and wide counting functions. Multiple DSPs can also be cascaded to construct larger mathematical functions, DSP filters and complex operations.

The main features of the DSP module include:

• 25×18 two's-complement multiplier

• 48bit accumulator

• Low-power pre-adder

• Single-instruction multiple-data arithmetic unit

• Arbitrary-function logic unit

• Pattern detector

• Optional pipeline and dedicated bus cascading

Table 49. DSP module application scenarios

No.	Internal module function
1	25-bit pre-adder (with or without D flip-flop)
2	25 x 18 multiplier
3	A, B, C, D data ports
4	Three-input adder/subtractor/48-bit logic operation unit
5	PATTERN detector
6	Pipeline function
7	DSP cascade function

7.2.2.6 Clock routing module

PL clock resources have dedicated global clocks, regional IO and clock resources. The clock management unit (CMT) provides clock frequency synthesis, deskew and jitter filtering. The use of non-clock resources (such as local routing) is not recommended when designing clock functions.

• The global clock tree allows clock resources for synchronous logic to span the module.

• IO and regional clock trees can drive up to 3 adjacent vertical clock regions.

• Each CMT contains one mixed-mode clock manager (MMCM) and one phase-locked loop (PLL), located close to the IO module column.

• For clocks, the PL can be divided into multiple clock regions.

• The number of clock regions is related to the PL device model; EKT7Z045 has 3 clock regions.

• The clock region includes all synchronous modules (such as CLB, IO, serial transceivers, DSP, BRAM, CMT), spanning 50 CLBs and one IO bank in a region, with a horizontal clock channel (HROW) in the middle.

• Each clock region is divided into 25 CLBs above HROW and 25 CLBs below HROW, symmetrically distributed with respect to HROW.

Each IO Bank contains clock-capable input pins (CC), to introduce user clocks into PL clock-routing resources. In conjunction with dedicated clock buffers, the clock-capable input pins bring user clocks to:

• Global clock lines in the same upper/lower half of the device

• IO clock lines in the same IO Bank and vertically adjacent IO Banks

• Regional clock lines in the same clock region and vertically adjacent clock regions

• CMTs in the same clock region and, with limitations, vertically adjacent clock regions

Devices all have 32 global clock lines that can provide clock and control signals to all timing resources throughout the device. The global clock buffer (BUFGCTRL, referred to as BUFG) drives global clock lines and must be used to access them. Each clock region supports up to 12 global clock lines using the 12 horizontal clock lines in the clock region.

Global clock buffers:

• Can be used as clock-enable circuitry to enable or disable multiple clock regions

• Can be used as glitch-free multiplexers to:
– Select between two clock sources
– Isolate unused clock sources

• Usually driven by CMTs to:
– Eliminate clock distribution delay
– Adjust clock delay relative to another clock

In a single clock region, the horizontal clock buffer (BUFH/BUFHCE) allows access to global clock lines through horizontal clock routing. It can also be used as clock-enable circuitry (BUFHCE) to independently enable or disable clocks spanning a single clock region. Each clock region can use 12 horizontal clock lines to support up to 12 clocks.

Within a clock region, each PL has regional and IO clock trees that can provide clocks to all timing resources. Each device also has multi-clock-region buffers (BUFMR), allowing regional and IO clocks to span three vertically adjacent clock regions.

• The IO clock buffer (BUFIO) drives the IO clock tree, providing clocks to all IO resources in the same IO bank.

• The regional clock buffer (BUFR) drives the regional clock tree, can drive all clock nodes in the same clock region, and can be programmed to divide the input clock frequency.

• In coordination with programmable serializers/deserializers in IOBs (see PL IO Resources User Guide), BUFIO and BUFR clock buffers allow source-synchronous systems to cross clock regions without using additional logic resources.

• Regional clock trees and IO clock trees of adjacent clock regions and IO Banks can be driven through a multi-clock-region buffer (BUFMR) when using associated BUFRs or BUFIOs.

• A clock region supports up to four independent regional clocks; an IO Bank supports up to four independent IO clocks.

• High-performance clock paths (HPC) connect certain specific CMT outputs directly to IO; these are direct paths with low jitter and minimal duty-cycle distortion.

Table 50. Main clock routing resources

No.	Module internal resources
1	Global clock buffer BUFG
2	IO clock buffer BUFIO
3	Clock region buffer BUFR
4	Multi-clock-region buffer BUFMR
5	Horizontal clock buffer BUFH

7.2.2.7 CMT module

The clock management tile (CMT) provides very flexible high-performance clock control. Each CMT contains one mixed-mode clock management module (MMCM) and one phase-locked loop (PLL).

The MMCM and PLL can be used as frequency synthesizers for various frequencies and as jitter filters for external or internal clocks, as well as for clock deskew. The PLL is a subset of the MMCM functions. PL clock input connections allow multiple resources to provide reference clocks for the MMCM and PLL.

The PL MMCM has infinitely fine phase-shift capability in either direction for dynamic phase-shift mode. The MMCM also has a microcounter in the feedback path or in one output path to achieve additional granularity in frequency synthesis.

Table 51. Main CMT module functions

No.	Internal module function
1	MMCM fractional division (O division) function
2	MMCM divider cascade (CLKOUT4 divider and CLKOUT6 divider)
3	MMCM reference clock selection function
4	CMT internal feedback
5	MMCM/PLL dynamic reconfiguration
6	MMCM dynamic phase-shift function
7	CMT cascade (MMCM to MMCM cascade, PLL to PLL cascade)
8	MMCM/PLL frequency synthesis function (frequency-point sampling)
9	MMCM spread-spectrum clock generator (SSCG)

7.2.2.8 ADC module

The ADC module inside PL mainly consists of two 12-bit analog-to-digital converters (ADCs) with sampling rates up to 1MSPS, and associated on-chip sensors.

Table 52. Main ADC module functions

No.	Function	Mode
1	Sampling mode	Initial mode
2	Sampling mode	Single mode
3	Sampling mode	Continuous mode
4	Sampling mode	Single-channel mode
5	Sampling mode	Synchronous sampling mode
6	Sampling mode	Independent ADC mode
7	Sampling mode	Initial mode
8	Calibration function	ADC offset calibration enable
9	Calibration function	ADC offset and gain calibration enable
10	Calibration function	Supply voltage sensor calibration enable
11	Calibration function	Supply voltage offset and gain calibration enable
12	Alarm function	Overtemperature alarm enable

Table 52. Main ADC module functions (continued)

No.	Function	Mode
13	Alarm function	Temperature alarm enable
14	Alarm function	VCCINT alarm
15	Alarm function	VCCAUX alarm
16	Alarm function	VCCBRAM alarm
17	Alarm function	Combined alarm
18	Power-up/down function	ADC power-up
19	Power-up/down function	Invalid selection
20	Power-up/down function	ADC power-down
21	Clock division function	DCLK division
22	Averaging filter function	Averaging filter enable (calibration)
23	Averaging filter function	No averaging
24	Averaging filter function	Average 16 times
25	Averaging filter function	Average 64 times
26	Averaging filter function	Average 256 times
27	ADC channel	On-chip temperature
28	ADC channel	Supply VCCINT
29	ADC channel	Supply VCCAUX
30	ADC channel	Dedicated analog input
31	ADC channel	Reference VREFP
32	ADC channel	Reference VREFN
33	ADC channel	Supply VCCBRAM
34	ADC channel	Invalid channel
35	ADC channel	XADC calibration
36	ADC channel	Invalid channel
37	ADC channel	Auxiliary channels 0 to 15
38	Analog input function	Single-ended input mode
39	Analog input function	Differential input mode

7.2.2.9 Configuration module

The configuration circuitry is closely related to the PL product architecture, which directly determines the system composition implemented by the configuration circuitry. Its basic function is to write different data combinations into the SRAM array to control the internal logic circuits and fulfill the user-designed function. What PL can implement is determined by its configuration bitstream file (.bit file).

The PL side only supports JTAG/boundary-scan configuration mode.

Table 53. Main configuration module functions

No.	Internal module function
1	JTAG/boundary-scan configuration
2	eFUSE (checkbit test data programming and reading)

7.2.2.10 GTX module

Each high-speed serial interface SERDES module contains a transmitter and a receiver and is divided into two parts: a physical coding sublayer (PCS) and a physical medium attachment sublayer (PMA). The PCS mainly implements data encoding, decoding and various protocol-control functions, while the PMA mainly implements parallel-to-serial and serial-to-parallel data conversion.

Table 54. Main SERDES module functions

Category	Function
PCS	2,4-byte internal data path to support different line-rate requirements
PCS	8B/10B encoding/decoding
PCS	Supports 64B/66B and 64B/67B encoding/decoding
PCS	Comma detection, byte and word alignment
PCS	PRBS generation and detection
PCS	TX phase FIFO
PCS	RX elastic FIFO for clock correction and channel bonding
PCS	Programmable logic interface
PCS	Supports 100Gb CAUI
PCS	Supports local multiple channels bypassing buffer
PCS	TX phase interpolation structure supports PPM Controller interface
PMA	Each QUAD shares QPLL, providing excellent jitter performance
PMA	Each channel is configured with one CPLL, providing a convenient clocking solution
PMA	High-efficiency adaptive linear equalization technology in low-power mode (LPM)
PMA	7tap decision feedback equalizer with adaptive adjustment
PMA	TX pre-emphasis
PMA	Adjustable TX output swing
PMA	Beacon signal for PCIE applications
PMA	OOB signal for SATA applications
PMA	Data rate support up to 8 Gbps (not full device operating temperature range)

The main application modes supported by high-speed serial transceivers are:

- PCI Express Gen1.1, 2.1
- 10GBASE-R
- Interlaken
- 10 Gb XAUI, RxAUI, 100 Gb CAUI, 40 Gb XLAUI
- CPRI™/ OBSAI

• OC-48/192
• OTU-1, OTU-2, OTU-3, OTU-4
• SRIO
• SATA/ SAS
• SDI

Table 55. Main SERDES-supported protocols, rates and internal data widths (using CPLL)

Protocol	Data rate (Gb/s)	Data width (16/20/32/40b)
XAUI	3.125	20b
XAUI	1.25	20b
Gigabit Ethernet	1.25	20b
RXAUI	6.25	20b
Aurora	6.25	20b
Aurora	5	20b
Aurora	3.125	20b
Aurora	2.5	20b
Aurora	1.25	20b
Serial RapidIO	3.125	20b
Serial RapidIO	2.5	20b
Serial RapidIO	1.25	20b
PCIe	5	20b
PCIe	2.5	20b
CPRI 1-10X	6.144	20b
CPRI 1-10X	4.9152	20b
CPRI 1-10X	3.072	20b
CPRI 1-10X	2.4576	20b
CPRI 1-10X	1.2288	20b
CPRI 1-10X	0.6144	20b
OBSAI	6.144	20b
OBSAI	3.072	20b
OBSAI	1.536	20b
OBSAI	0.768	20b
3G-SDI HD-SDI	2.97	20b
3G-SDI HD-SDI	1.485	20b
Interlaken	6.25	16b
Interlaken	4.25	16b
Interlaken	3.125	16b
SFI-5	3.125	16b
OC-48	2.48832	16b

Table 55. Main SERDES-supported protocols, rates and internal data widths (using CPLL) (continued)

Protocol	Data rate (Gb/s)	Data width (16/20/32/40b)
OC-12	0.62208	16b
OTU-1	2.666057	16b
SATA/SAS	6	20b
SATA/SAS	3	20b
SATA/SAS	1.5	20b
CPRI 1-4X	2.4576	20b
CPRI 1-4X	1.2288	20b
CPRI 1-4X	0.6144	20b
Fibre Channel	4.25	20b
Fibre Channel	2.125	20b
Fibre Channel	1.0625	20b

Table 56. Main SERDES-supported protocols, rates and internal data widths (using QPLL)

Protocol	Data rate (Gb/s)	Data width (16/20/32/40b)
PCIe Gen2	5	32b

• Digital algorithm implements automatic calibration of 50-ohm termination impedance;

• PLL frequency lock detection implemented by digital algorithm;

• TX supports configurable de-emphasis and output differential voltage amplitude;

• RX supports continuous-time linear equalization (CTLE) and decision feedback equalization (DFE), as well as low-power mode operation;

• Uses second-order digital clock and data recovery (CDR) based on phase interpolation;

• Built-in digital eye-diagram scan function, including horizontal and vertical scanning;

• Multiple loopback paths (far-end and near-end loopback on PMA and PCS sides), built-in self-test modes (PRBS7, PRBS15, PRBS23 and PRBS31), and PMA internal signal testing.

7.2.2.11 PCIE module

The PCIE module supports PCIE Gen2, x1, x2, x4 and x8; the module specifies a data rate of 5.0Gbps per lane.

Table 57. Main PCIE2_1 module functions

No.	Category / internal module function	Details
1	User interface	AXI4-Stream interface 64bit, 128bit, 256bit
2	Link width	X1, X2, X4, X8
3	Link rate	2.5Gb/s, 5.0Gb/s
4	DRP	Dynamically reconfigurable
5	Power control	Power management
6	Transfer mode	Requester/completer dual-channel transfer
7	Protocol layer — Generate and process transaction-layer packets	Memory-type packet read, write, completion (with data, without data)

Table 57. Main PCIE2_1 module functions (continued)

No.	Category / internal module function	Details
8	Protocol layer — Generate and process transaction-layer packets	Configuration-type packet read, write, completion (with data, without data)
9	Protocol layer — Generate and process transaction-layer packets	Message-type packet read, write, completion (with data, without data)
10	Protocol layer — Packet transfer	Flow control management
11	Protocol layer — Packet transfer	Interrupts up to 32 MSI and MSI-X vectors
12	Protocol layer — Packet transfer	Supports INTx
13	Protocol layer — Packet transfer	Maximum transfer payload 1024bytes
14	Protocol layer — Packet transfer	Transaction ordering
15	Protocol layer — Link training state machine	Lane reversal
16	Protocol layer — Link training state machine	Link initialization
17	Protocol layer — Link training state machine	Link training
18	Protocol layer — Link training state machine	Link maintenance
19	Protocol layer — Link training state machine	Link negotiation handshake
20	Configuration management	Type 0/1 configuration header area
21	Configuration management	Configuration space access
22	Configuration management	PCIE extended capability space
23	Configuration management	Loopback control and status
24	Configuration management	Error reporting and status
25	Configuration management	Device serial number extension
26	Configuration management	Device ID capture and storage
27	Configuration management	User-defined configuration capability

8. Application recommendations

8.1 Development tool version

The recommended version of the PL development tool is Vivado 2018.3; for SOC development software, SDK 2018.3 or Vitis 2019.2 is recommended.

8.2 PL power-up sequencing requirements

Note: The power-up and power-down requirements must be followed. Failure to follow the power-up requirements may cause erroneous programming of efuse in the PL circuit and irreversible damage to the device!!!

Power-up requirements:

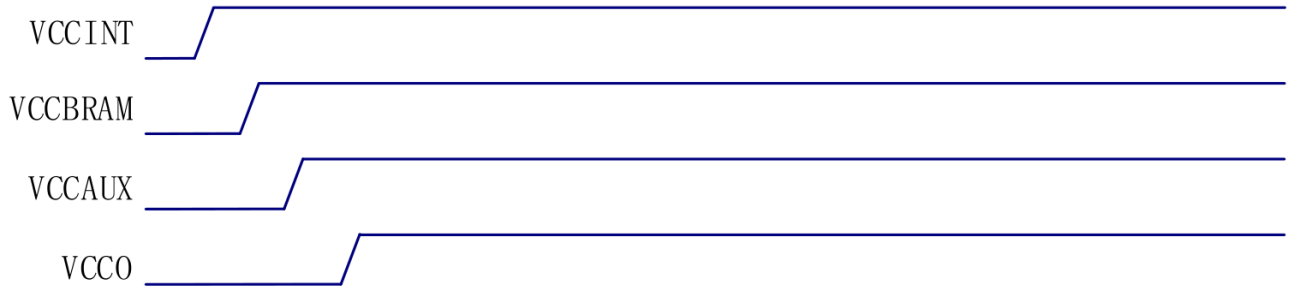


Figure 17. PL power-up requirements

8.3 PS power-up and power-down sequencing requirements

Note: The power-up and power-down requirements must be followed. Failure to follow the power-up and power-down requirements may cause erroneous programming of efuse in the PS circuit and irreversible damage to the device!!!

Power-up requirements:

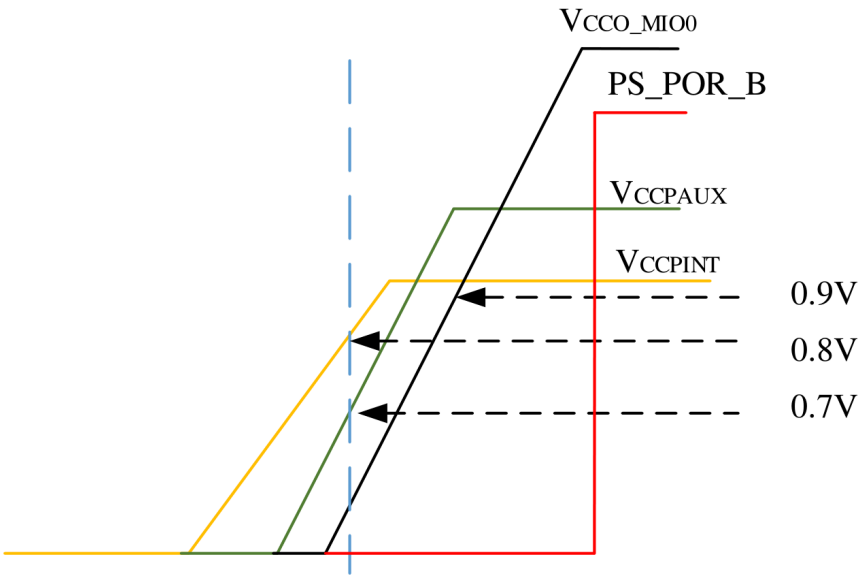


Figure 18. PS power-up requirements

Power-down requirements:

Power-down may meet either PS power-down requirement 1 or requirement 2.

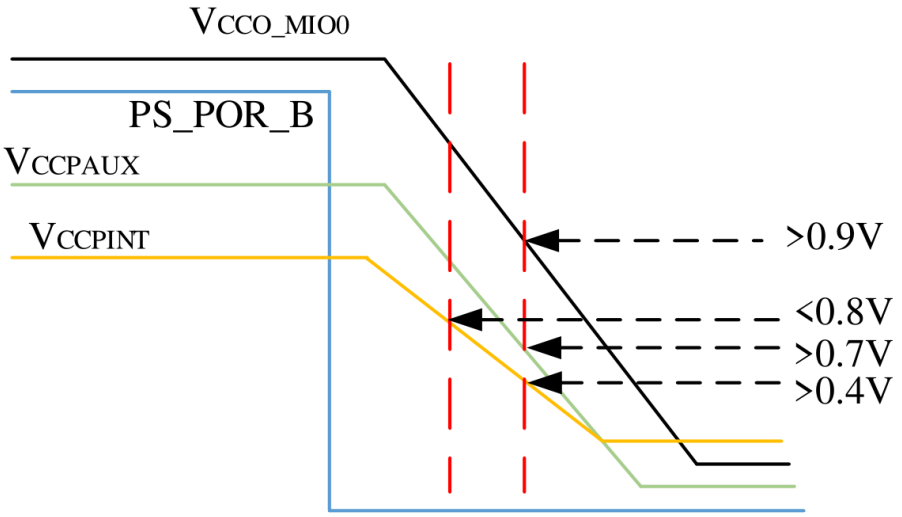


Figure 19. PS power-down requirement 1

Or

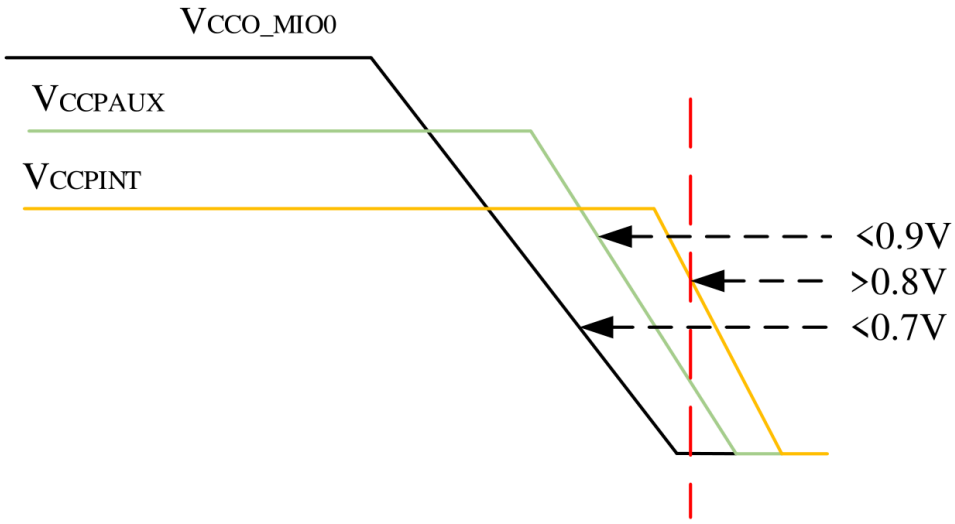


Figure 20. PS power-down requirement 2

8.4 Development flow

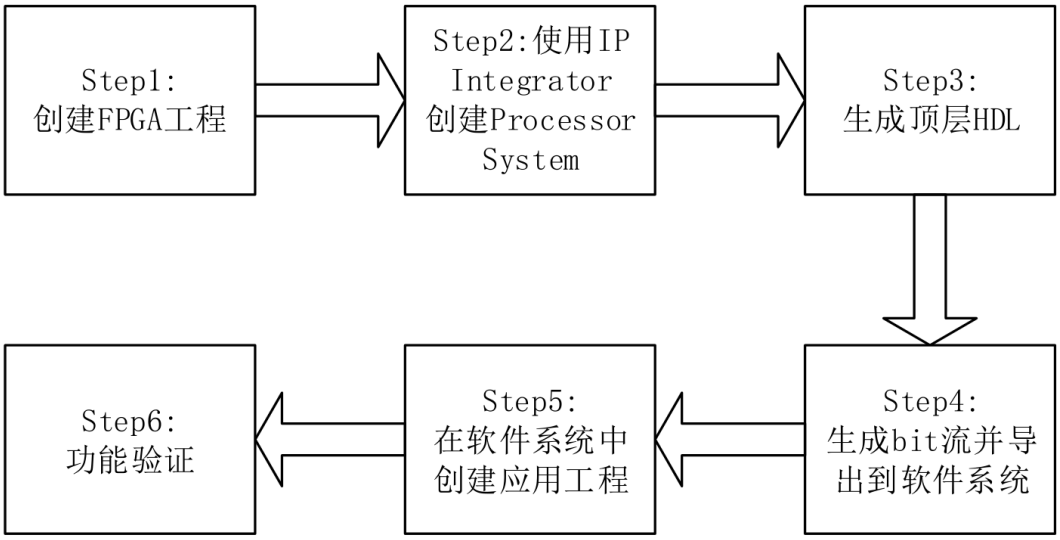


Figure 21. EKT7Z045 development flow

Diagram steps: Step 1: Create an FPGA project; Step 2: Use IP Integrator to create the Processor System; Step 3: Generate top-level HDL; Step 4: Generate the bitstream and export it to the software system; Step 5: Create an application project in the software system; Step 6: Functional verification.

As shown above, the development flow can be broadly divided into 6 steps. Step 1 through Step 4 are the hardware design part and are implemented in Vivado software; Step 5 is the software design part, implemented in SDK software; Step 6 is functional verification. Complex programs also involve Debug, which is also implemented in SDK software.

The PS-side boot flow is shown in the following figure:

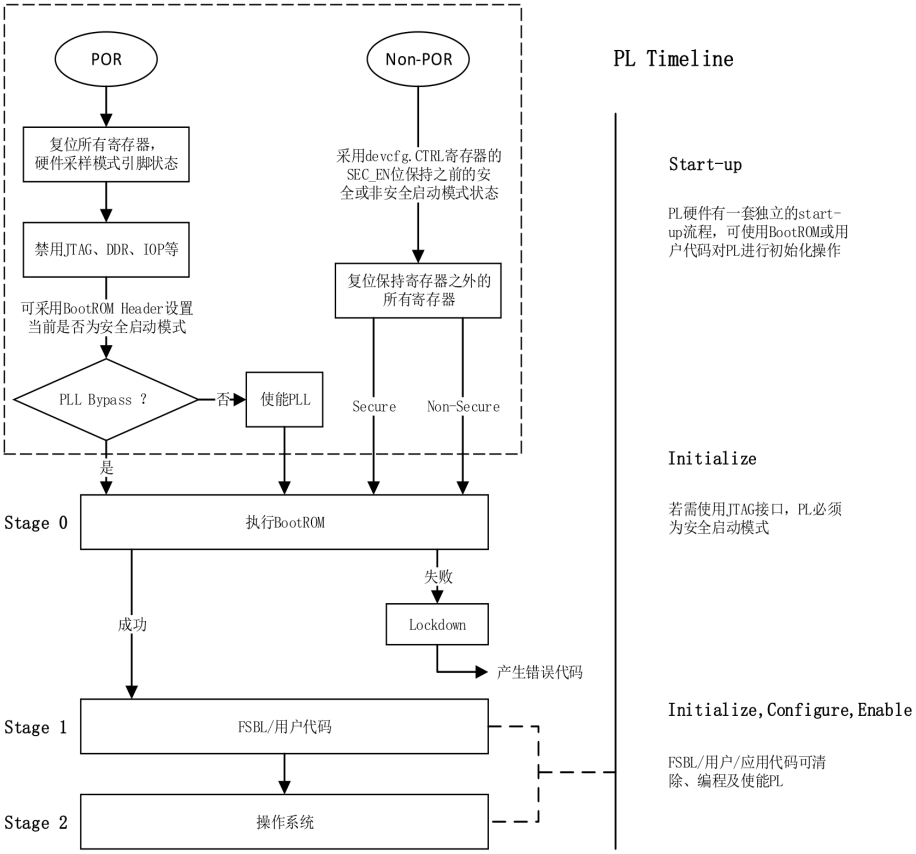


Figure 22. EKT7Z045 boot flow

Diagram labels: POR: reset all registers, hardware samples boot mode pin state; disable JTAG, DDR, IOP, etc.; BootROM Header can set whether current boot mode is secure; PLL Bypass? Yes / No; enable PLL. Non-POR: use SEC_EN bit of devcfg.CTRL register to retain previous secure or non-secure boot mode state; reset all registers except retention registers. Stage 0: Execute BootROM; success / failure; Lockdown; generate error code. Stage 1: FSBL/user code. Stage 2: Operating system. PL timeline: Start-up: PL hardware has an independent start-up process; BootROM or user code can initialize PL. Initialize: if JTAG interface is needed, PL must be in secure boot mode. Initialize, Configure, Enable: FSBL/user/application code can clear, configure and enable PL.

Hardware boot phase

The PS hardware boot phase includes supply voltage ramp rate, clock, reset, pin sampling and PLL initialization. The PL can be powered up when the PS starts.

External PS control pins

Within 45 clock cycles of the PS_CLK reference clock, hardware samples the seven boot-mode pins and stores their settings in read-only registers. The pins define the initial voltage sensitivity of the MIO input buffers, select the JTAG chain routing and select the Flash device containing the boot image. The development board automatically pulls the PS_POR_B reset pin low after power-up. The board also includes a POR reset button to generate a POR reset. The PS_SRST_B reset pin can be used to generate a non-POR system reset.

PS PLL initialization

The PS PLL is enabled by the MIO[6](BOOT_MODE[4]) pin. When the PLL is enabled, execution of BootROM is delayed until the PLL output locks. If the PLL is not enabled, the PS_CLK reference clock input pin bypasses the PLL and the clock subsystem is driven at the frequency of the PS_CLK input.

PS software boot phase

The PS software boot process is controlled by BootROM and FSBL/user code. BootROM code operation is affected by the boot pins, BootROM Header and the contents detected by BootROM code in the system.

Stage 0 (BootROM: BootROM Header)

After power-on reset (POR) or non-POR system reset (PS_SRST_B, debug, watchdog, software), hard-coded BootROM executes on the primary CPU (CPU0). BootROM reads the BootROM Header programmed into the boot Flash device to determine the boot flow and transition to Stage 1. After the hardware boot sequence, both CPUs begin executing the same BootROM code at address 0x0 (the initial location of BootROM) to determine their own characteristics. Note that a single-core device contains one processor, and a dual-core device contains two. When CPU1 is present, it pauses itself by executing the WFE instruction. CPU0 continues to execute BootROM.

Stage 1 (FSBL/user code)

This is usually the first-stage boot loader, but it can be any user-controlled code.

Stage 2 (U-Boot/system/application)

This is usually system software, but it may also be a second-stage boot loader (SSBL).

During power-on boot and configuration, EKT7Z045 first reads the external mode pin levels to determine the configuration mode, then completes PS-side configuration through internal BootROM and boot code. If the PL side is not configured through JTAG, it must be configured by the PS side. The EKT7Z045 configuration key pins are shown in the following table:

Table 58. Configuration key pins

Pin name	I/O type	PS side / PL side	Description
PS_POR_B	Input	PS side	POR reset pin, the only reset that reads the pull-up/pull-down state of boot-mode pins. For the power-up sequence, set the PS_POR_B input low until VCCPINT, VCCPAUX and VCCO_MIO0 reach the minimum operating level, to ensure the integrity of PS eFUSE.
PS_SRST_B	Input	PS side	Non-POR reset pin for forcing system reset. It can be floating or pulled up, and may be high during PS-side power-up.
MIO[2]	Inout	PS side	After PS_POR_B is pulled low, the system reads this pin pull-up/pull-down state and writes it into a register to determine the JTAG chain connection mode. 0: Cascaded mode; 1: Independent mode. Note: In secure mode, JTAG is not enabled and the pin state is ignored.
MIO[5:3]	Inout	PS side	After PS_POR_B is pulled low, the system reads this pin pull-up/pull-down state and writes it into a register to determine the configuration mode. 000: JTAG; 001: NOR; 010: NAND; 100: QSPI; 110: SD card.
MIO[6]	Inout	PS side	After PS_POR_B is pulled low, the system reads this pin pull-up/pull-down state and writes it into a register to determine whether the PLL is enabled. 0: Enable PLL. The system waits for PLL lock, then executes BootROM; 1: Bypass PLL to support a wider PS_CLK frequency range.

Table 58. Configuration key pins (continued)

Pin name	I/O type	PS side / PL side	Description
MIO[8:7]	Inout	PS side	After PS_POR_B is pulled low, the system reads this pin pull-up/pull-down state and writes it into a register to determine the port voltage standards used by BANK_500 and BANK_501. 00: BANK_500 and BANK_501 port voltage is 2.5V or 3.3V; 01: BANK_500 port voltage is 1.8V, BANK_501 port voltage is 2.5V or 3.3V; 10: BANK_500 port voltage is 2.5V or 3.3V, BANK_501 port voltage is 1.8V; 11: BANK_500 and BANK_501 port voltage is 1.8V. Note: If an interface uses MIO on both BANKs, the voltage standards of the two BANKs must be consistent.
CFGBVS	Input	PL side	Configuration BANK (BANK0) voltage selection. When CFGBVS is high, BANK0 voltage is 2.5V or 3.3V; when CFGBVS is low, BANK0 voltage is ≤ 1.8V. CFGBVS must be tied high or low; floating is not permitted. If other BANKs participate in configuration, their port voltage must match BANK0.
TCK	Input	PL side	IEEE Std 1149.1 (JTAG) Test clock pin for connecting to the programmer TCK pin, implementing program download, upload and online debugging. A weak pull-down resistor (e.g. 1KΩ) is recommended to keep TCK low when no programmer is connected.
TMS	Input	PL side	IEEE Std 1149.1 (JTAG) Test mode select pin for connecting to the programmer TMS pin, implementing program download, upload and online debugging. A weak pull-up resistor (e.g. 4.7KΩ) is recommended to keep TMS high when no programmer is connected.
TDI	Input	PL side	IEEE Std 1149.1 (JTAG) Test data input pin. A weak pull-up resistor (e.g. 4.7KΩ) is recommended. For a single device, connect to the programmer TDI pin. When multiple devices form a JTAG daisy chain, connect the first device to the programmer TDI pin; otherwise connect to the preceding device TDO pin. Used for program download, upload and online debugging.
TDO	Output	PL side	IEEE Std 1149.1 (JTAG) Test data output pin. A weak pull-up resistor (e.g. 4.7KΩ) is recommended. For a single device, connect to the programmer TDO pin. When multiple devices form a JTAG daisy chain, connect the last device to the programmer TDO pin; otherwise connect to the next device TDI pin. Used for program download, upload and online debugging.
PROGRAM_B	Input	PL side	When PROGRAM_B generates a low pulse, it clears PL-side configuration and allows the PS side or the JTAG TAP controller to configure the PL side. PROGRAM_B must be connected through a ≤ 4.7KΩ pull-up resistor to VCCO_0 to ensure a stable high input.
INIT_B	Inout	PL side	INIT_B is 0 before initialization is complete or when a configuration error occurs. After PL initialization is complete, INIT_B is released to high Z, and an external resistor pulls INIT_B high. • INIT_B is open-drain and can be used for wired-AND logic; • If INIT_B is held low, the power-on configuration sequence can be paused after initialization is complete; INIT_B must be connected through a ≤ 4.7KΩ pull-up resistor to VCCO_0.
DONE	Inout	PL side	Configuration sequence completion flag. High indicates configuration completion. DONE is open-drain; a 10K pull-up resistor is integrated in the circuit, but an external 330Ω pull-up to VCCO_0 is still recommended.

In addition to JTAG mode, EKT7Z045 supports the following configuration modes:

(1) NOR mode

(2) NAND mode

(3) QSPI mode

(4) SD card mode

The programming mode pins (MIO5, MIO4, MIO3) select the programming mode. The mode selection codes are shown below.

Table 59. Programming mode coding [1],[2],[3],[4] — Boot mode

Pin signal	MIO8	MIO7	MIO6	MIO5	MIO4	MIO3	MIO2
JTAG				0	0	0	JTAG chain: 0: Cascaded mode; 1: Independent mode
NOR				0	0	1	JTAG chain: 0: Cascaded mode; 1: Independent mode
NAND				0	1	0	JTAG chain: 0: Cascaded mode; 1: Independent mode
QSPI				1	0	0	JTAG chain: 0: Cascaded mode; 1: Independent mode
SD				1	1	0	JTAG chain: 0: Cascaded mode; 1: Independent mode

PLL mode

Pin signal	MIO6	Description
PLL enable	0	Hardware waits for PLL lock, then executes ROM boot
PLL bypass	1	Wider PS_CLK frequency range

MIO Bank voltage

Voltage	Bank1 (MIO8)	Bank0 (MIO7)	Description
2.5V, 3.3V	0	0	Voltage Bank0 contains MIO0 to MIO15; voltage Bank1 contains MIO16 to MIO53
1.8V	1	1	Voltage Bank0 contains MIO0 to MIO15; voltage Bank1 contains MIO16 to MIO53

Note 1: JTAG cascaded mode is most common, and is the default mode in all descriptions of JTAG mode.

Note 2: In secure mode, JTAG is not enabled and MIO2 is ignored.

Note 3: Quad SPI and NOR boot modes support the execute-in-place function (this support is always in non-secure mode).

Note 4: If an interface spans these two voltage BANKs, both BANKs must be set to the same voltage.

8.5 NOR mode

NOR mode boot requires an 8-bit asynchronous NOR FLASH memory device with a maximum capacity of 256Mb. The reference configuration diagram is shown below:

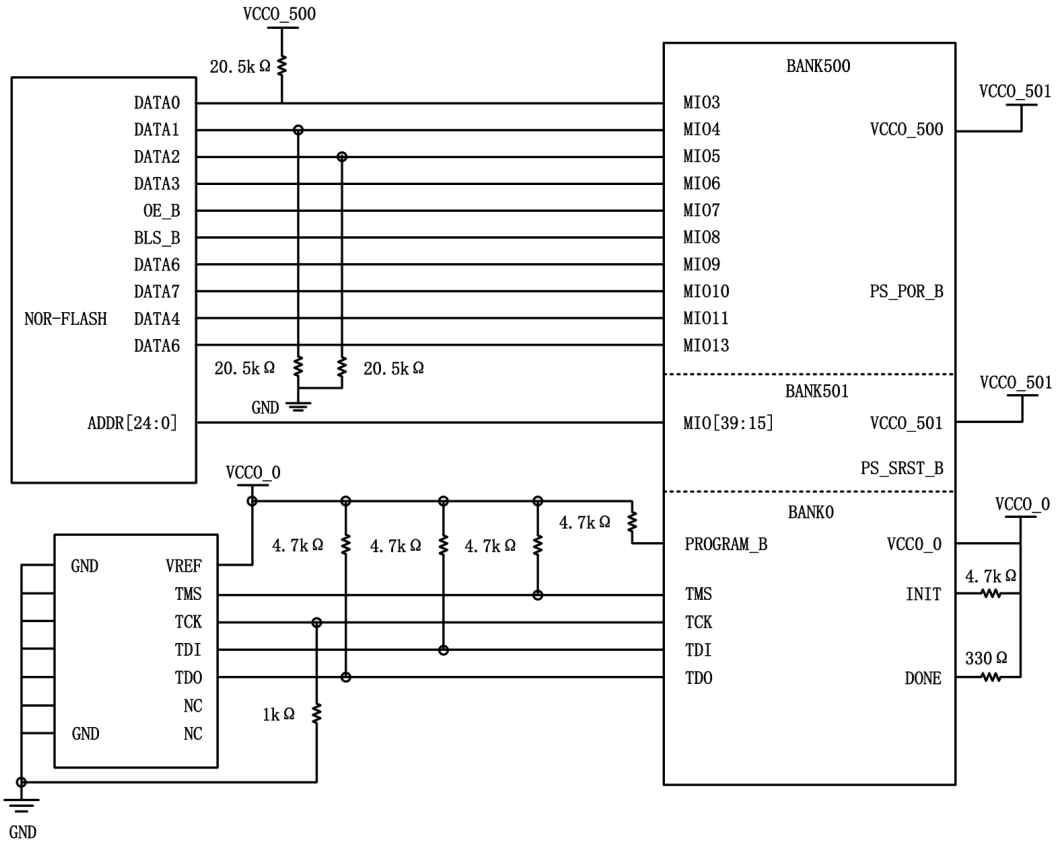


Figure 23. Mode configuration schematic

When using NOR mode, note the following:

(1) During power-up, the PS_SRST_B low-to-high transition must precede the PS_POR_B low-to-high transition by at least 2us;

(2) NOR mode occupies pins on both BANK_500 and BANK501, so port levels of the two BANKs must be consistent;

(3) PL VCCO_0 and programmer VREF must have the same voltage;

(4) The DONE pin is an open-drain output. A 330Ω pull-up resistor is recommended;

(5) The INIT_B pin is a bidirectional open-drain pin. An external pull-up resistor is required;

(6) PROGRAM_B also requires a pull-up resistor;

(7) VCCBATT is the supply for the AES key stored in SRAM. When used, it should be connected to the battery supply.

8.6 NAND mode

For NAND mode boot, select an 8-bit or 16-bit NOR FLASH memory device supporting the ONFI 1.0 protocol. The reference configuration diagram is shown below:

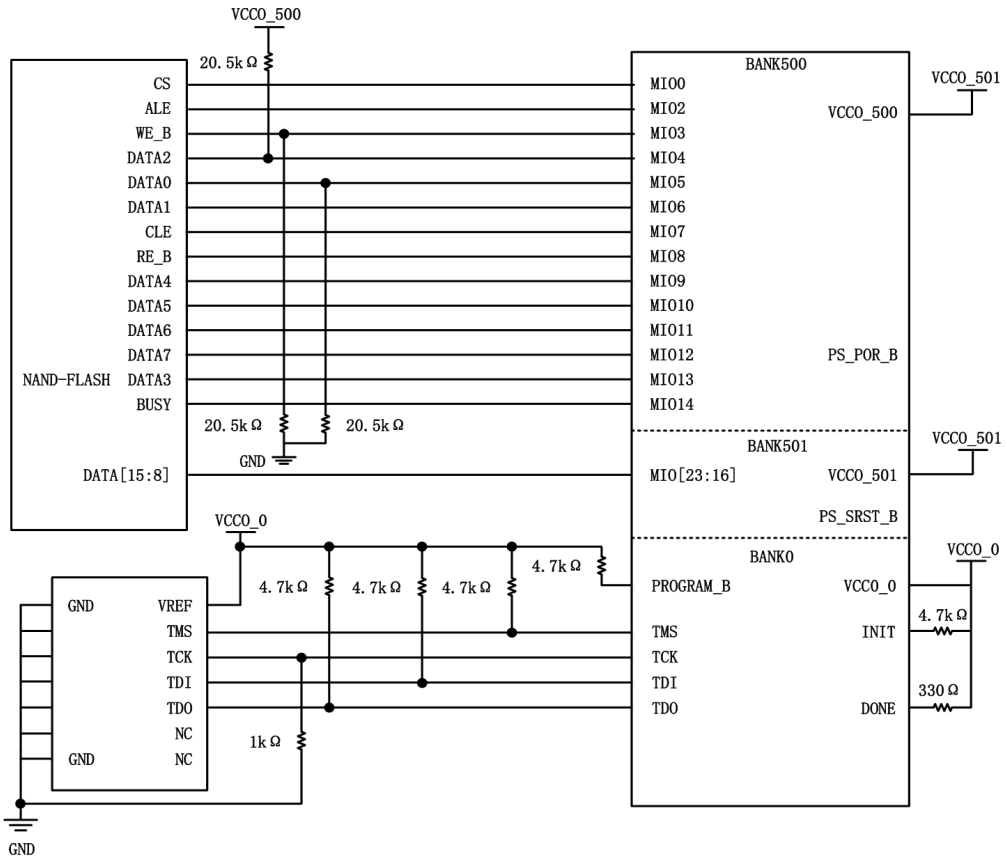


Figure 24. NAND mode configuration schematic

When using NAND mode, note the following:

(1) During power-up, the PS_SRST_B low-to-high transition must precede the PS_POR_B low-to-high transition by at least 2us;

(2) NAND mode occupies pins on both BANK_500 and BANK501, so port levels of the two BANKs must be consistent;

(3) The boot image must be placed in the first 128Mb of address space for the BootROM header search function;

(4) PL VCCO_0 and programmer VREF must have the same voltage;

(5) The DONE pin is an open-drain output. A 330Ω pull-up resistor is recommended;

(6) The INIT_B pin is a bidirectional open-drain pin. An external pull-up resistor is required;

(7) PROGRAM_B also requires a pull-up resistor;

(8) VCCBATT is the supply for the AES key stored in SRAM. When used, it should be connected to the battery supply.

8.7 QSPI mode

In QSPI mode, a single QSPI FLASH device with 1-bit, 2-bit or 4-bit width can be selected for configuration, supporting a configuration memory space of 16MB. Alternatively, dual QSPI FLASH devices can be selected to form an 8-bit I/O parallel configuration mode, or dual QSPI FLASH devices can form a 4-bit I/O stacked configuration mode. Dual QSPI FLASH supports a configuration memory space of 32MB. The configuration reference diagrams are shown below:

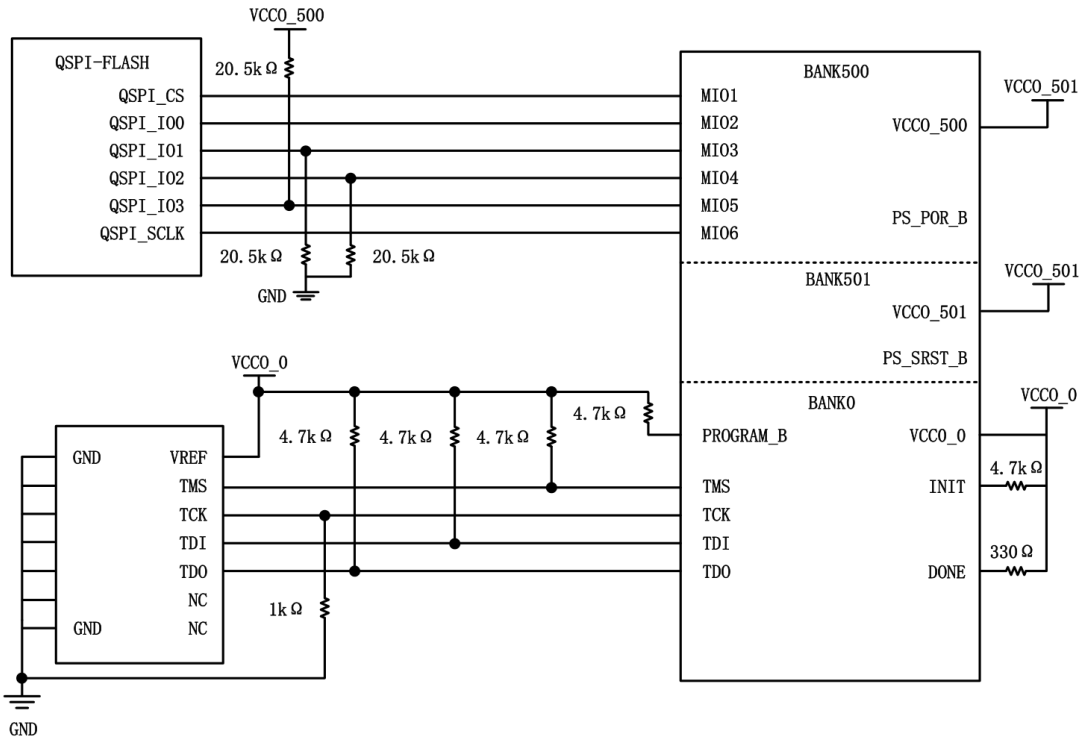


Figure 25. Single QSPI mode configuration schematic

The reference diagram for the dual QSPI FLASH 8-bit parallel configuration is shown below. The configuration address space increases from 16MB to 32MB (24-bit address to 25-bit address), and data throughput doubles.

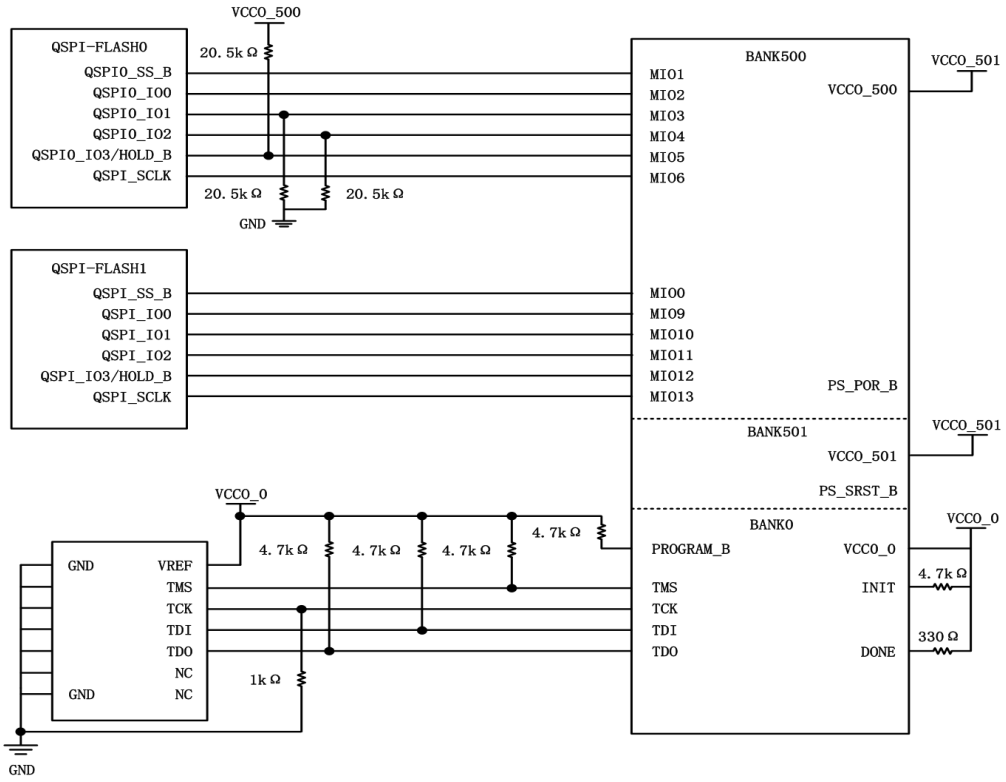


Figure 26. Dual QSPI 8-bit parallel configuration schematic

The reference diagram for the dual QSPI FLASH 4-bit stacked configuration is shown below. The configuration address space increases from 16MB to 32MB (24-bit address to 25-bit address), saving pin routing space. Data throughput is the same as that of a single QSPI, and execute-in-place is not supported.

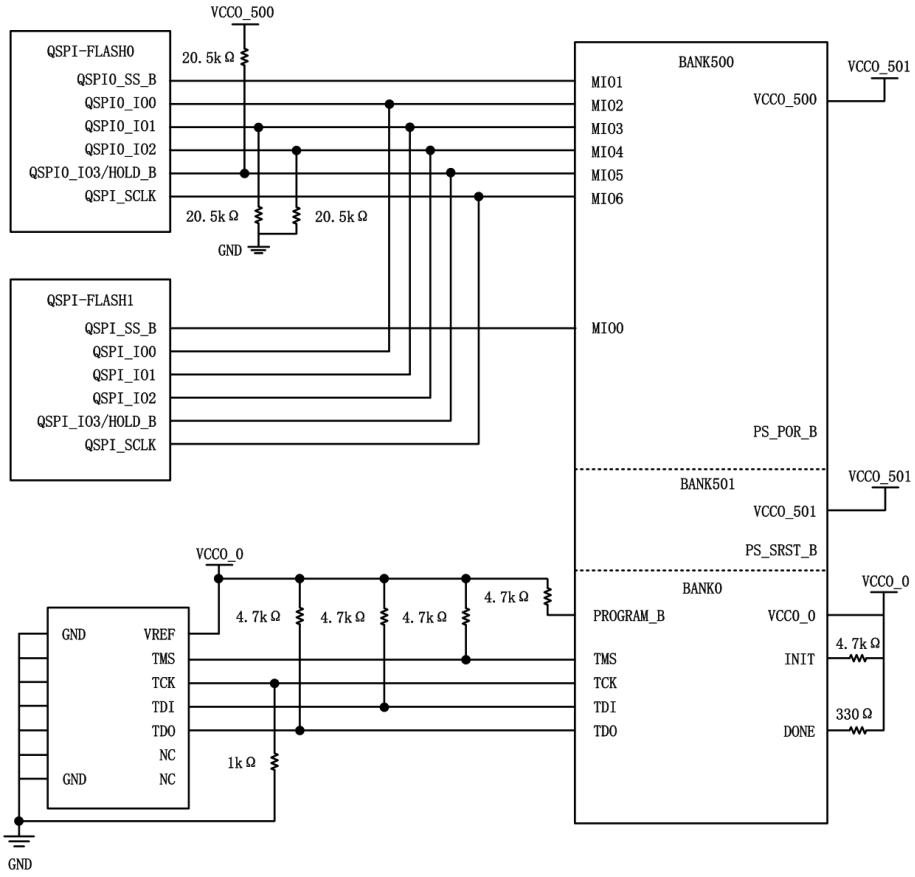


Figure 27. Dual QSPI 4-bit stacked configuration schematic

When using QSPI mode, note the following:

(1) During power-up, the PS_SRST_B low-to-high transition must precede the PS_POR_B low-to-high transition by at least 2us;

(2) PL VCCO_0 and programmer VREF must have the same voltage;

(3) The DONE pin is an open-drain output. A 330Ω pull-up resistor is recommended;

(4) The INIT_B pin is a bidirectional open-drain pin. An external pull-up resistor is required;

(5) PROGRAM_B also requires a pull-up resistor;

(6) VCCBATT is the supply for the AES key stored in SRAM. When used, it should be connected to the battery supply.

8.8 SD card mode

SD card mode reads configuration data from an SD card. FAT16/32 file systems are supported, with a maximum SD card capacity of 32GB. The configuration reference diagram is shown below:

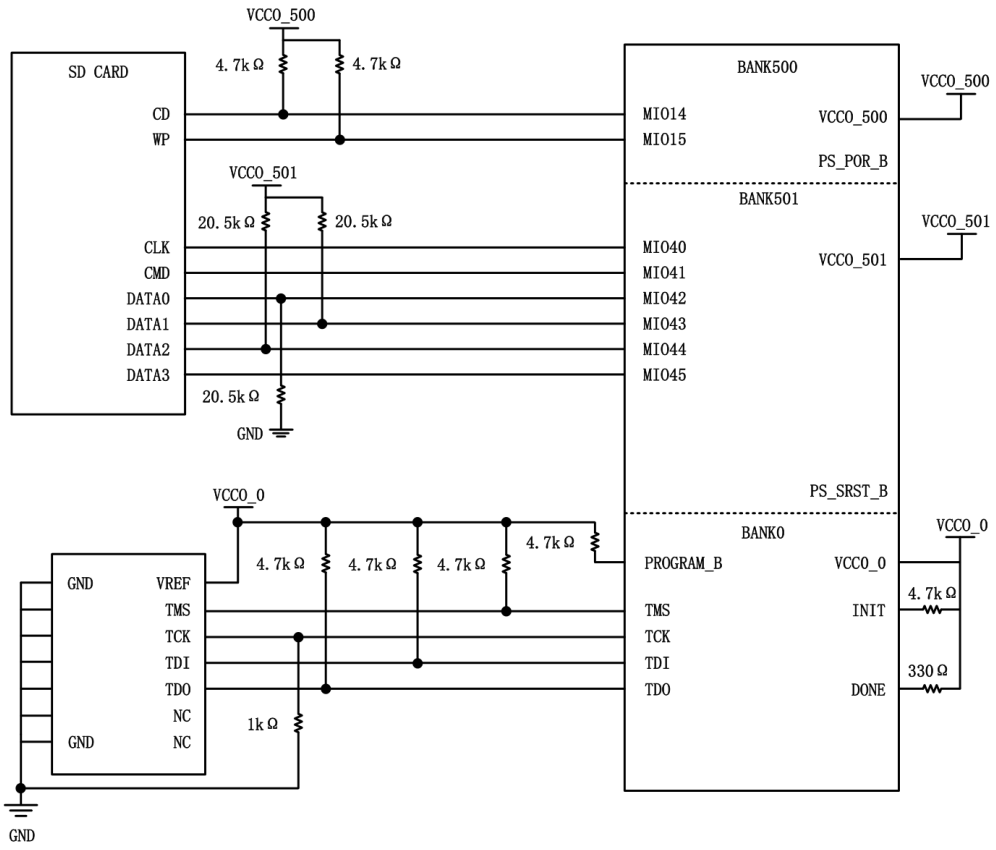


Figure 28. SD card mode configuration schematic

When using SD card mode, note the following:

(1) During power-up, the PS_SRST_B low-to-high transition must precede the PS_POR_B low-to-high transition by at least 2us;

(2) If CD (Card Detect), WP (Write Protect) pins, etc. are required, these pins must be pulled up;

(3) PL VCCO_0 and programmer VREF must have the same voltage;

(4) The DONE pin is an open-drain output. A 330Ω pull-up resistor is recommended;

(5) The INIT_B pin is a bidirectional open-drain pin. An external pull-up resistor is required;

(6) PROGRAM_B also requires a pull-up resistor;

(7) VCCBATT is the supply for the AES key stored in SRAM. When used, it should be connected to the battery supply.

8.9 SerDes (GTX) application precautions

EKT7Z045 uses a forward benchmarking design approach, so GTX application differs from AMD devices.

8.9.1 AVCC/AVTT power supply requirements

The SerDes AVCC must be independently powered. Sharing with other supplies is not recommended (in particular, it must not share VCCINT), to avoid noise from other power supplies affecting performance. The ripple at the AVCC pin must be less than 10mVpp, and the voltage including ripple must strictly remain within the recommended operating conditions.

AVTT should likewise be supplied independently. Sharing with other supplies is not recommended. The ripple at the AVTT pin must be less than 10mVpp, and the voltage including ripple must strictly remain within the recommended operating conditions.

8.9.2 Reference clock requirements

The differential peak-to-peak input amplitude at the reference clock pin is 350mV–2000mV, and random jitter must be less than 1ps (rms).

AC coupling capacitors should be placed near the FPGA device.

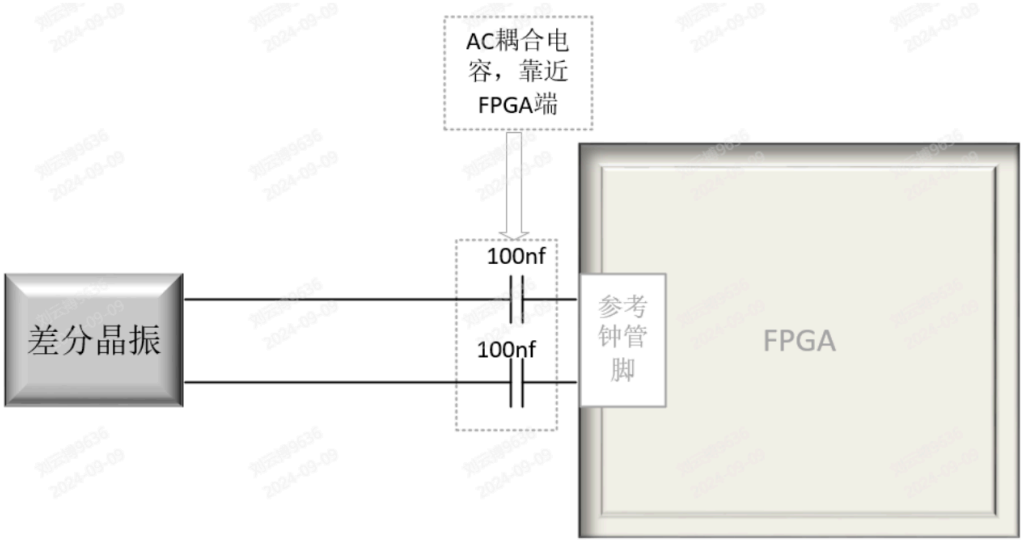


Figure 29. Reference clock AC coupling capacitor placement

Diagram labels: Differential crystal oscillator; AC coupling capacitors close to FPGA; reference clock pins.

The main functions of AC coupling are:

- Disconnect DC components between devices to reduce power consumption;
- Maintain independent common-mode voltages;
- The capacitor and termination resistance form a high-pass filter, reducing the baseline drift of the clock.

8.9.3 Lane coupling capacitor placement

The location of the lane coupling capacitors should be determined according to the relevant protocol user guide.

8.9.4 PCB high-speed signal routing

To avoid crosstalk, the spacing between adjacent PCB traces for the SerDes reference clock and TX/RX high-speed signals should be at least three times the trace width.

8.9.5 Termination resistor calibration design

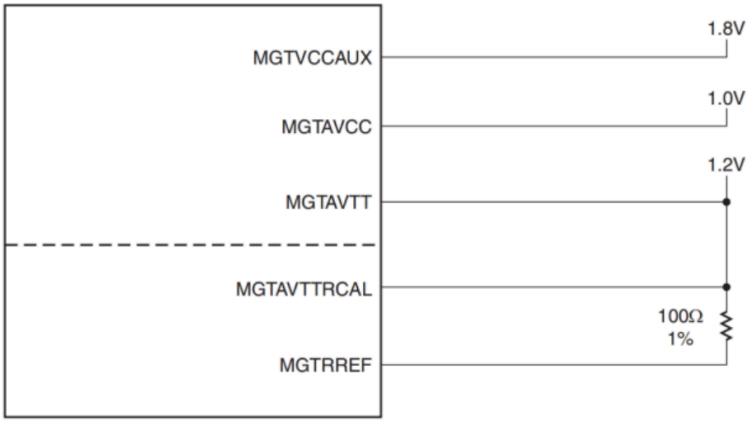


Figure 30. Termination resistor calibration schematic

MGTAVTTRCAL is the power supply for the termination resistor calibration module, and MGTRREF is the calibration resistor input. Connect the MGTAVTTRCAL pin to the MGTAVTT supply and one terminal of a 100Ω precision external resistor, and connect the other terminal to MGTRREF. The PCB traces from MGTAVTTRCAL and MGTRREF to the corresponding terminals of the resistor must be equal in length.

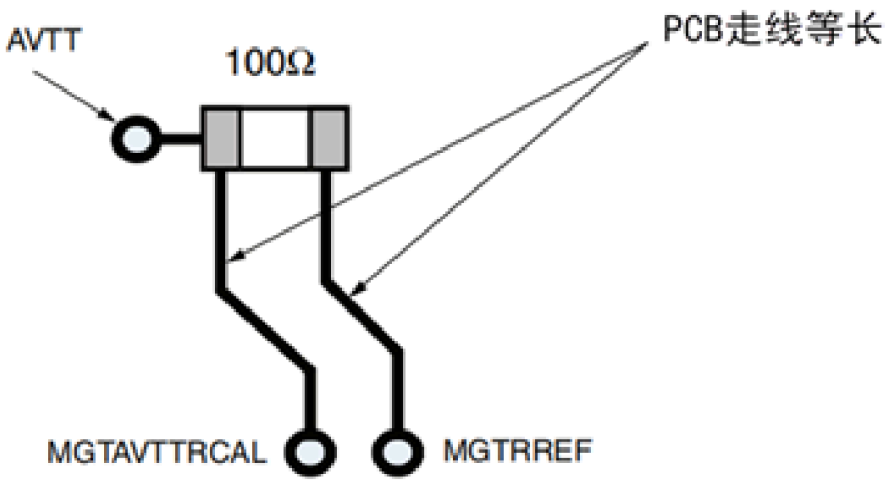


Figure 31. RCAL resistor PCB layout

Diagram label: PCB traces of equal length.

8.9.6 IBERT GTX IP digital eye diagram compatibility

To use the IBERT GTX IP digital eye diagram function, modify the underlying Vivado CSV file. The file path is: XILINX\Vivado\2018.3\data\xicom\ibert_slave_k7gtx_channel.csv .

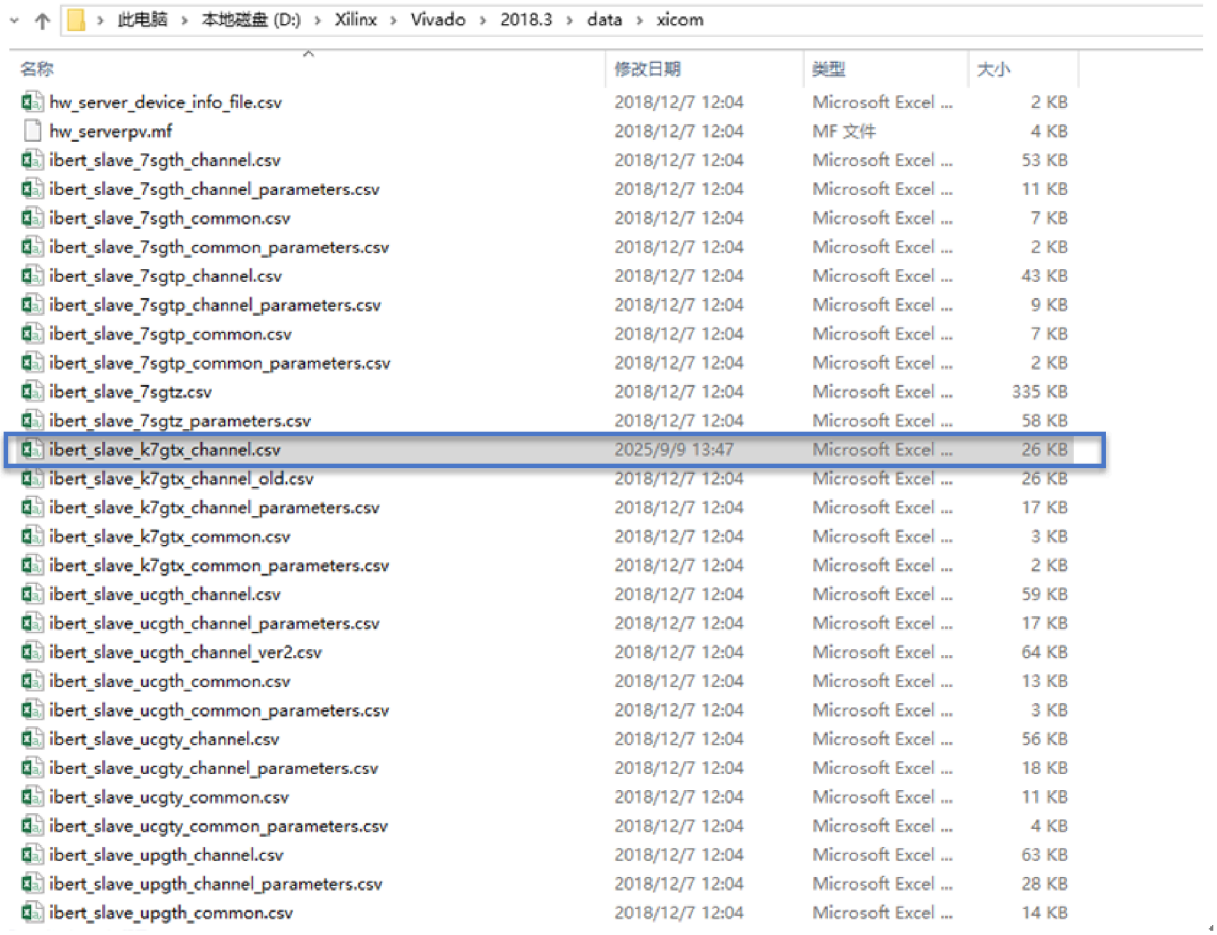


Figure 32. CSV file location

Modify rows 232–244 of the CSV file by adding 2 in hexadecimal to each value, as shown below.

Figure 33. CSV file modification contents

Row	Register	Before (hex)	After (hex)
232	DRP.ES_ERROR_COUNT	14F	151
233	DRP.ES_SAMPLE_COUNT	150	152
234	DRP.ES_CONTROL_STATUS	151	153
235	DRP.ES_RDATA	156	158
236	DRP.ES_RDATA	155	157
237	DRP.ES_RDATA	154	156
238	DRP.ES_RDATA	153	155
239	DRP.ES_RDATA	152	154
240	DRP.ES_SDATA	15B	15D
241	DRP.ES_SDATA	15A	15C

Figure 33. CSV file modification contents (continued)

Row	Register	Before (hex)	After (hex)
242	DRP.ES_SDATA	159	15B
243	DRP.ES_SDATA	158	15A
244	DRP.ES_SDATA	157	159

After modification, start Vivado and download the bit file of the IBERT demo project. The digital eye diagram function can be used normally.

Note: This modification causes the digital eye diagram function of Xilinx devices to operate abnormally. Back up the original file before modification.

8.9.7 QPLL VCO bandwidth compatibility

The Xilinx GTX QPLL VCO range is segmented into 5.93GHz–8.0GHz and 9.8GHz–12.5GHz. The EKT7Z045 QPLL VCO range is continuous from 6.8GHz to 12.5GHz. Thus operation of QPLL from 5.93GHz to 6.8GHz (including divided intervals such as 2 and 4) with Xilinx default settings is not supported by EKT7Z045. It is recommended to use CPLL below 6.8GHz. The following describes the QPLL modification method.

PLL output frequency formula:

F_PLLClkout = F_PLLClkin × N / (M × 2) (1)

PLL output frequency formula:

F_LineRate = F_PLLClkout × 2 / D (2)

Table 60. QPLL division settings

Coefficient	Attribute	Valid values
M	QPLL_REFCLK_DIV	1, 2, 3, 4
N	QPLL_FBDIV; QPLL_FBDIV_RATIO	16, 20, 32, 40, 64, 66, 80, 100
D	RXOUT_DIV / TXOUT_DIV	1, 2, 4, 8, 16

Table 61. Coefficient N settings

N	QPLL_FBDIV_RATIO	QPLL_FBDIV
16	1	0000100000
20	1	0000110000
32	1	0001100000
40	1	0010000000
64	1	0011100000
66	0	0101000000
80	1	0100100000
100	1	0101110000

As shown in the table above, for the incompatible QPLL range, the QPLL compatibility problem can be resolved by doubling the PLL output frequency (N × 2) and then doubling the TX/RX division coefficient (D × 2).

Note: (1) The above modification applies only to a typical clock at a specific frequency.

(2) In theory, the user can configure the QPLL coefficients according to formulas 1 and 2 above. However, it is not recommended to set M to a value other than 1.

The table below lists recommended PLL settings for supported GTX protocols. Incompatible protocols and frequency points are shown explicitly as not compatible (bold italic in the original).

Table 62. PLL recommendations for EKT7Z045FFG900 GTX protocols

Protocol	Rate Gb/s	PLL out GHz	Ref. MHz	PLL mode	Xilinx compat.	TX/RX D	CPLL M	CPLL N2	CPLL N1	QPLL M	QPLL N
Fibre Channel (single rate)	4.25	2.125	212.5	CPLL	Yes	1	1	2	5	-	-
Fibre Channel (single rate)	2.125	2.125	106.25	CPLL	Yes	2	1	4	5	-	-
Fibre Channel (single rate)	1.0625	2.125	106.25	CPLL	Yes	4	1	4	5	-	-
Fibre Channel (multi-rate)	4.25	2.125	212.5	CPLL	Yes	1	1	2	5	-	-
Fibre Channel (multi-rate)	2.125	2.125	212.5	CPLL	Yes	2	1	2	5	-	-
Fibre Channel (multi-rate)	1.0625	2.125	212.5	CPLL	Yes	4	1	2	5	-	-
XAUI	3.125	3.125	156.25	CPLL	Yes	2	1	4	5	-	-
XAUI	3.125	12	156.25	QPLL	No	4	-	-	-	1	80
XAUI	6.25	3.125	156.25	CPLL	Yes	1	1	4	5	-	-
XAUI	6.25	12	156.25	QPLL	No	2	-	-	-	1	80
RXAUI	6.25	3.125	156.25	CPLL	Yes	1	1	4	5	-	-
RXAUI	6.25	12	156.25	QPLL	No	2	-	-	-	1	80
GigE	1.25	2.5	125	CPLL	Yes	1	1	4	5	-	-
Aurora (single rate)	6.25	3.125	312.5	CPLL	Yes	1	1	2	5	-	-
Aurora (single rate)	5	2.5	250	CPLL	Yes	1	1	2	5	-	-
Aurora (single rate)	3.125	3.125	156.25	CPLL	Yes	2	1	4	5	-	-
Aurora (single rate)	2.5	2.5	125	CPLL	Yes	2	1	4	5	-	-
Aurora (single rate)	1.25	2.5	125	CPLL	Yes	4	1	4	5	-	-
Aurora (multi-rate)	6.25	3.125	312.5	CPLL	Yes	1	1	2	5	-	-
Aurora (multi-rate)	5	2.5	312.5	CPLL	Yes	1	1	2	4	-	-
Aurora (multi-rate)	3.125	3.125	312.5	CPLL	Yes	2	1	2	5	-	-
Aurora (multi-rate)	2.5	2.5	312.5	CPLL	Yes	2	1	2	4	-	-
Aurora (multi-rate)	1.25	2.5	312.5	CPLL	Yes	4	1	2	4	-	-
Aurora 64B/66B	3.125	3.125	156.25	CPLL	Yes	2	1	4	5	-	-
Serial RapidIO (single rate)	3.125	3.125	156.25	CPLL	Yes	2	1	4	5	-	-
Serial RapidIO (single rate)	2.5	2.5	125	CPLL	Yes	2	1	4	5	-	-

Table 62. PLL recommendations for EKT7Z045FFG900 GTX protocols (continued)

Protocol	Rate Gb/s	PLL out GHz	Ref. MHz	PLL mode	Xilinx compat.	TX/RX D	CPLL M	CPLL N2	CPLL N1	QPLL M	QPLL N
Serial RapidIO (single rate)	1.25	2.5	125	CPLL	Yes	4	1	4	5	-	-
Serial RapidIO (multi-rate)	3.125	3.125	156.25	CPLL	Yes	2	1	4	5	-	-
Serial RapidIO (multi-rate)	2.5	2.5	156.25	CPLL	Yes	2	1	4	4	-	-
Serial RapidIO (multi-rate)	1.25	2.5	156.25	CPLL	Yes	4	1	4	4	-	-
SATA	6	3	150	CPLL	Yes	1	1	4	5	-	-
SATA	3	3	150	CPLL	Yes	2	1	4	5	-	-
SATA	1.5	3	150	CPLL	Yes	4	1	4	5	-	-
SATA	6	6	150	QPLL	No	2	-	-	-	1	80
SATA	3	6	150	QPLL	No	4	-	-	-	1	80
SATA	1.5	6	150	QPLL	No	8	1	-	-	1	80
PCIE	2.5	2.5	100	CPLL	Yes	2	1	5	5	1	80
PCIE	5	2.5	100	CPLL	Yes	1	1	5	5	1	80
PCIE	8	8	100	QPLL	Yes	1	-	-	-	1	80
CPRI (multi-rate)	3.072	3.072	122.88	CPLL	Yes	2	1	5	5	-	-
CPRI (multi-rate)	2.4576	2.4576	122.88	CPLL	Yes	2	1	4	5	-	-
CPRI (multi-rate)	1.2288	1.2288	122.88	CPLL	Yes	4	1	4	5	-	-
CPRI (multi-rate)	0.6144	0.6144	122.88	CPLL	Yes	8	1	4	5	-	-
CPRI (multi-rate)	9.8304	9.8304	122.88	QPLL	Yes	1	-	-	-	1	80
OBSAI (multi-rate)	6.144	3.072	153.6	CPLL	Yes	1	1	4	5	-	-
OBSAI (multi-rate)	3.072	3.072	153.6	CPLL	Yes	2	1	4	5	-	-
OBSAI (multi-rate)	1.536	3.072	153.6	CPLL	Yes	4	1	4	5	-	-
OBSAI (multi-rate)	0.768	3.072	153.6	CPLL	Yes	8	1	4	5	-	-
3G-SDIHD-SDI (multi-rate)	2.97	2.97	148.5	CPLL	Yes	2	1	4	5	-	-
3G-SDIHD-SDI (multi-rate)	1.485	2.97	148.5	CPLL	Yes	4	1	4	5	-	-
Interlaken	6.25	3.125	312.5	CPLL	Yes	1	1	2	5	-	-
Interlaken	4.25	3.125	212.5	CPLL	Yes	1	1	2	5	-	-
Interlaken	3.125	3.125	156.25	CPLL	Yes	2	1	4	5	-	-
Interlaken	10.3125	10.3125	161.13	QPLL	Yes	1	-	-	-	1	80
SFI-5	3.125	3.125	195.3125	CPLL	Yes	2	1	4	4	-	-
OC-48	2.48832	2.48832	155.52	CPLL	Yes	2	1	4	4	-	-
OC-12	0.62208	2.48832	155.52	CPLL	Yes	8	1	4	4	-	-
OTU-1	2.666057	2.666057	166.6286	CPLL	Yes	2	1	4	4	-	-
CEI 6.25	6.25	3.125	390.625	CPLL	Yes	1	1	2	4	-	-

Table 62. PLL recommendations for EKT7Z045FFG900 GTX protocols (continued)

Protocol	Rate Gb/s	PLL out GHz	Ref. MHz	PLL mode	Xilinx compat.	TX/RX D	CPLL M	CPLL N2	CPLL N1	QPLL M	QPLL N
CEI 6.25	6.25	12.5	390.625	QPLL	No	2	-	-	-	1	32
CEI 6.25	6.25	12.5	156.25	QPLL	No	2	-	-	-	1	80
10GBASE-R (156.25 MHz)	10.3125	10.3125	156.25	QPLL	Yes	1	-	-	-	1	66
OC-192 (9.953 Gb/s, 155.516 MHz)	9.953024	9.953024	155.516	QPLL	Yes	1	-	-	-	1	64
Standard: SFP+ (SFF-8431, SFI)	9.95328	9.95328	155.52	QPLL	Yes	1	-	-	-	1	64
Standard: SFP+ (SFF-8431, SFI)	10.3125	10.3125	156.25	QPLL	Yes	1	-	-	-	1	66
Standard: SFP+ (SFF-8431, SFI)	10.5187	10.3125	164.355	QPLL	Yes	1	-	-	-	1	64
Standard: SFP+ (SFF-8431, SFI)	11.1	11.1	173.4375	QPLL	Yes	1	-	-	-	1	64

Note 1: TX/RX division coefficient D attributes are TXOUT_DIV, RXOUT_DIV.

Note 2: CPLL coefficient M attribute is CPLL_REFCLK_DIV.

Note 3: CPLL coefficient N2 attribute is CPLL_FBDIV.

Note 4: CPLL coefficient N1 attribute is CPLL_FBDIV_45.

Note 5: QPLL coefficient M attribute is QPLL_REFCLK_DIV.

Note 6: QPLL coefficient N attributes are QPLL_FBDIV, QPLL_FBDIV_RATIO.

The following describes in detail the QPLL compatibility solutions for IP officially provided by Xilinx, based on the recommended values above.

(1) IBERT 7 Series GTX IP

The following describes the use of GTX at 3.125Gb/s in QPLL mode. Users can refer to this method to resolve IBERT incompatibility at other frequencies.

Step 1: Set the line rate to 3.125Gbps, the reference clock to 156.25MHz, and select Quad PLL, as shown below.

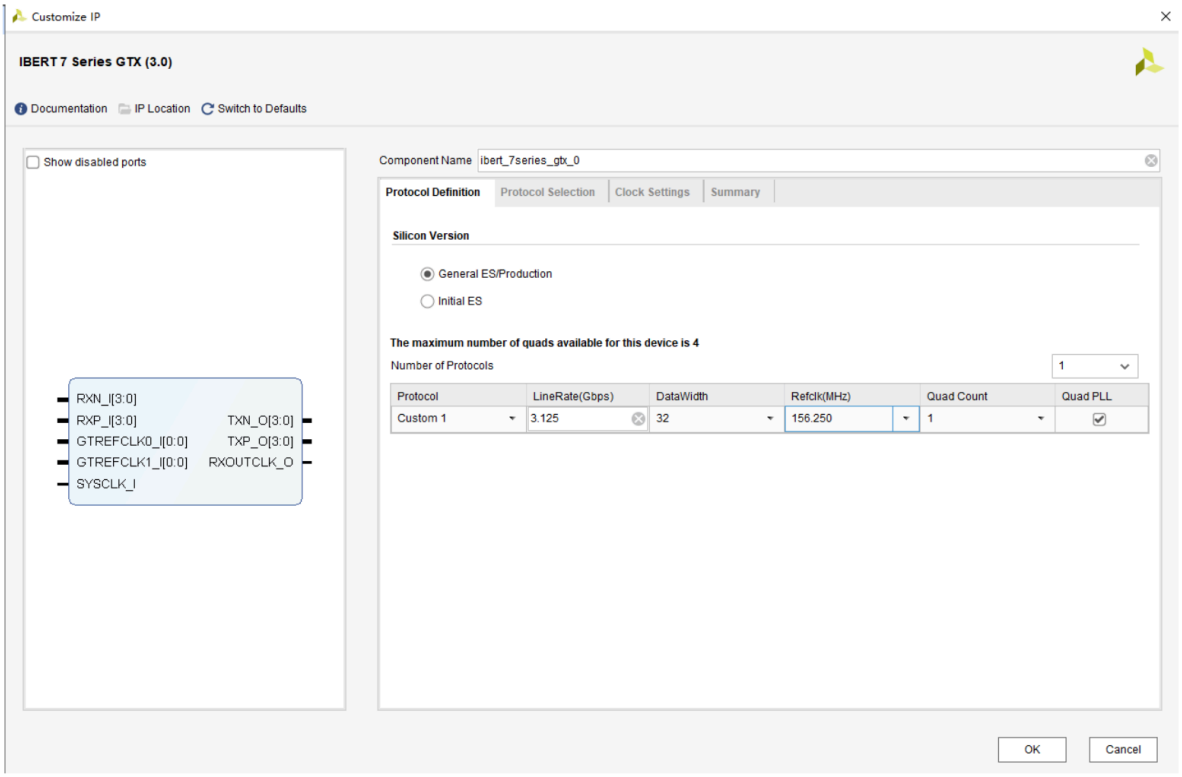


Figure 34. IBERT IP settings 1

Note: EKT7Z045 GTX supports only a 32bit data width.

Step 2: Set the QUAD location. The example below selects bank 115, with the GTX clock input from bank 115 clk0 (select according to the actual board requirements).

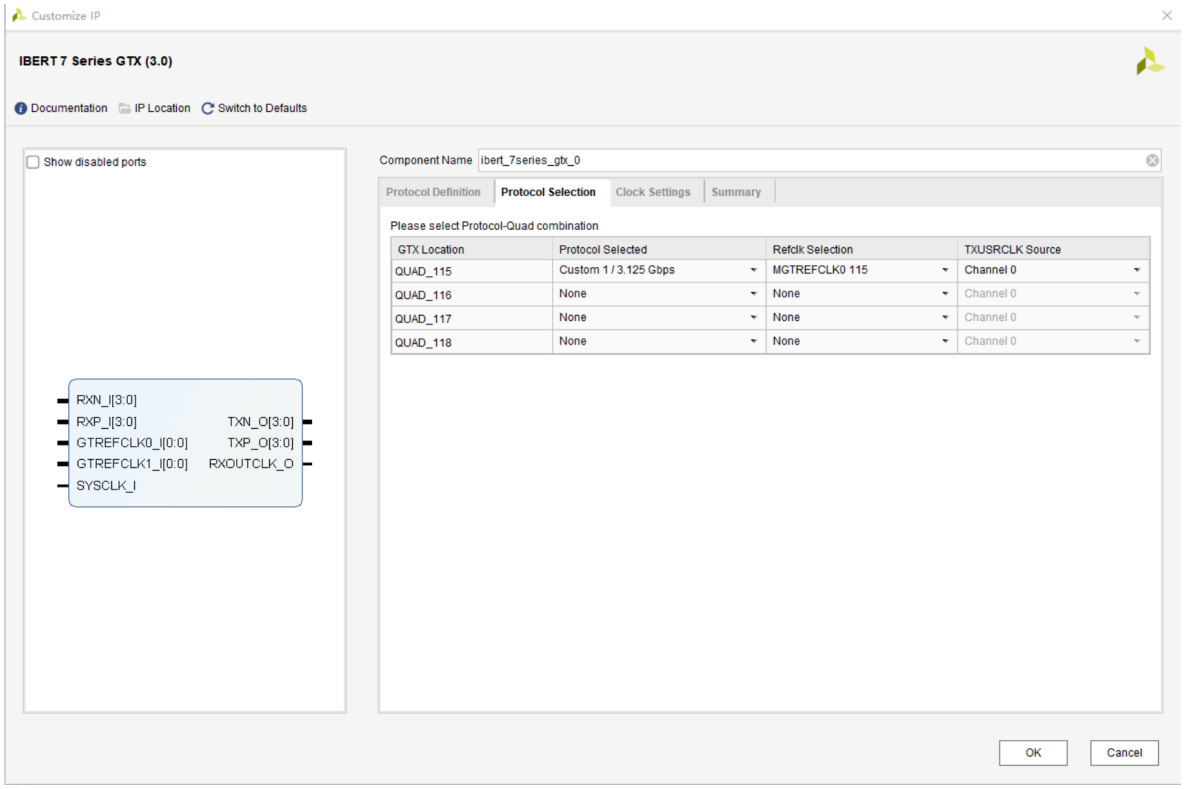


Figure 35. IBERT IP settings 2

Step 3: Set the IBERT IP CORE clock. In the example below, the GTX PHY reference clock is recommended to eliminate one differential clock input.

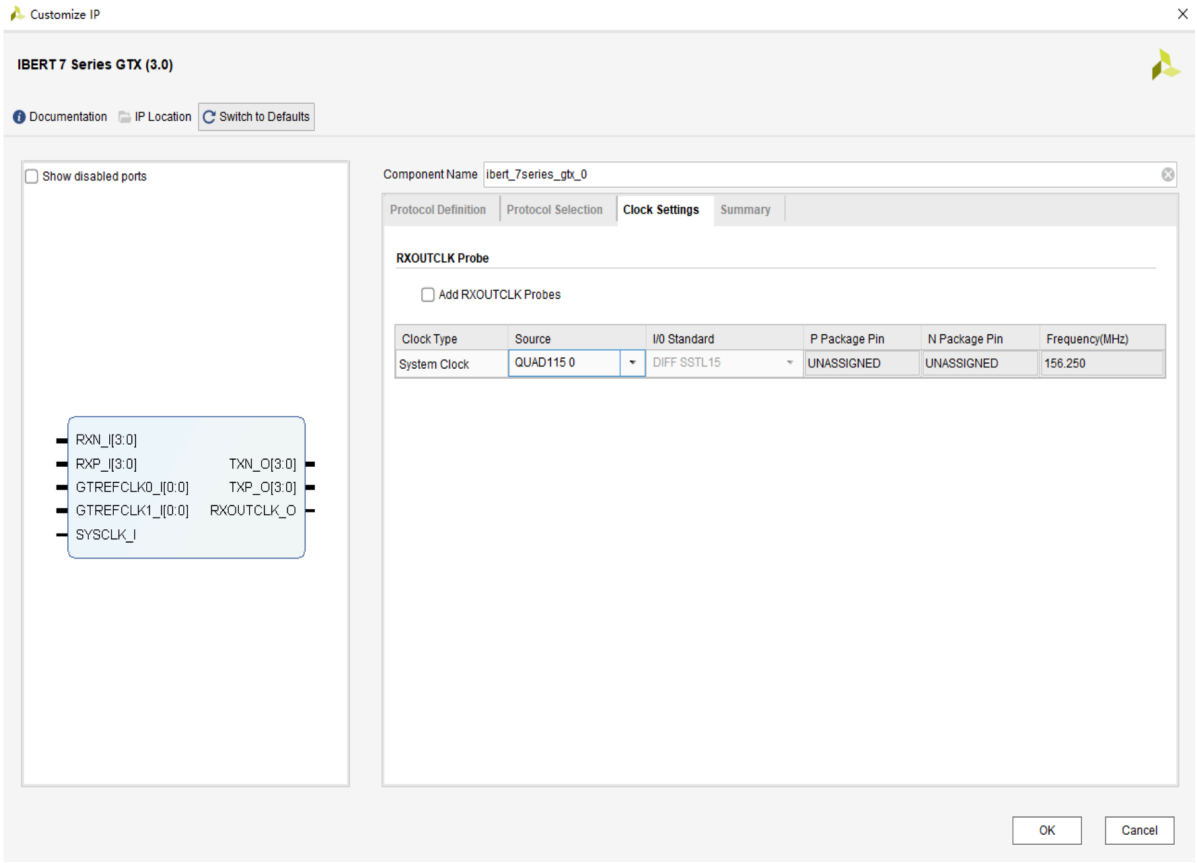


Figure 36. IBERT IP settings 3

Step 4: After configuring the settings, click OK to generate the IP. Then select IBERT IP and right-click Open IP Example Design, as shown below.

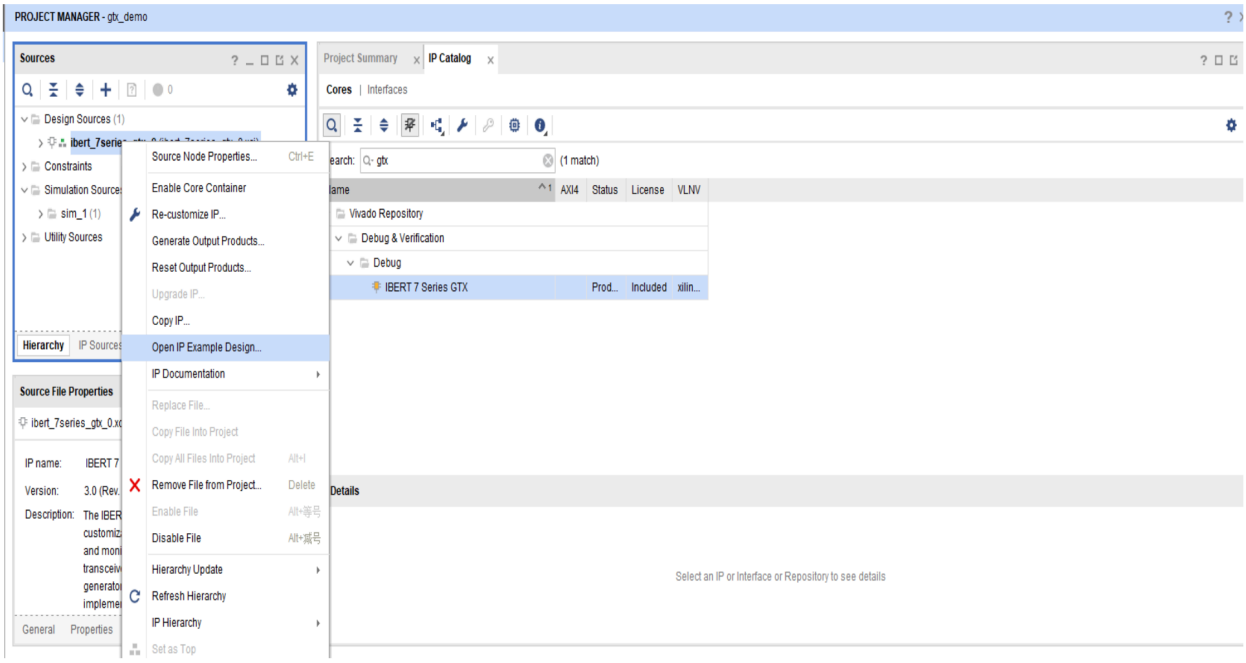


Figure 37. Open IBERT DEMO project

Step 5: Open the demo project XDC file and make the following modifications.

a. Add two QPLL constraints, as shown below.

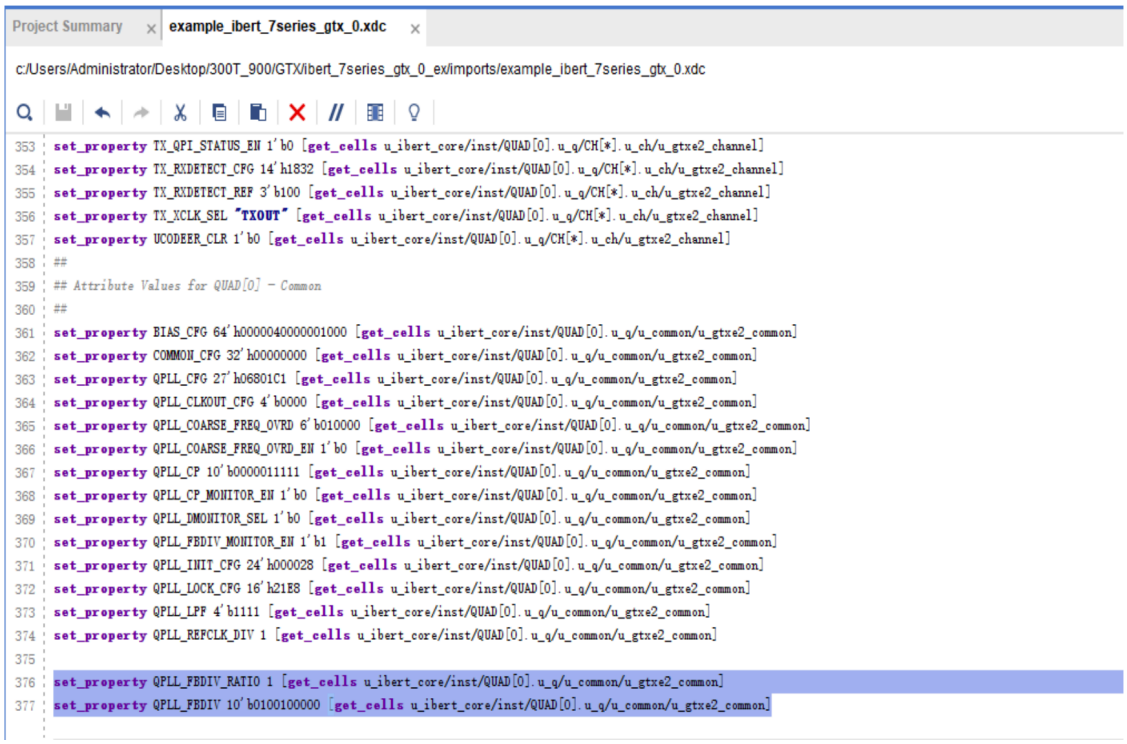


Figure 38. Add QPLL constraints

Set QPLL_FBDIV_RATIO to 1 and QPLL_FBDIV to 10’b0100100000 (i.e., set the M parameter to 80, as stated in the source).

b. Change TXOUT_DIV/RXOUT_DIV from 2 to 4, as shown below.

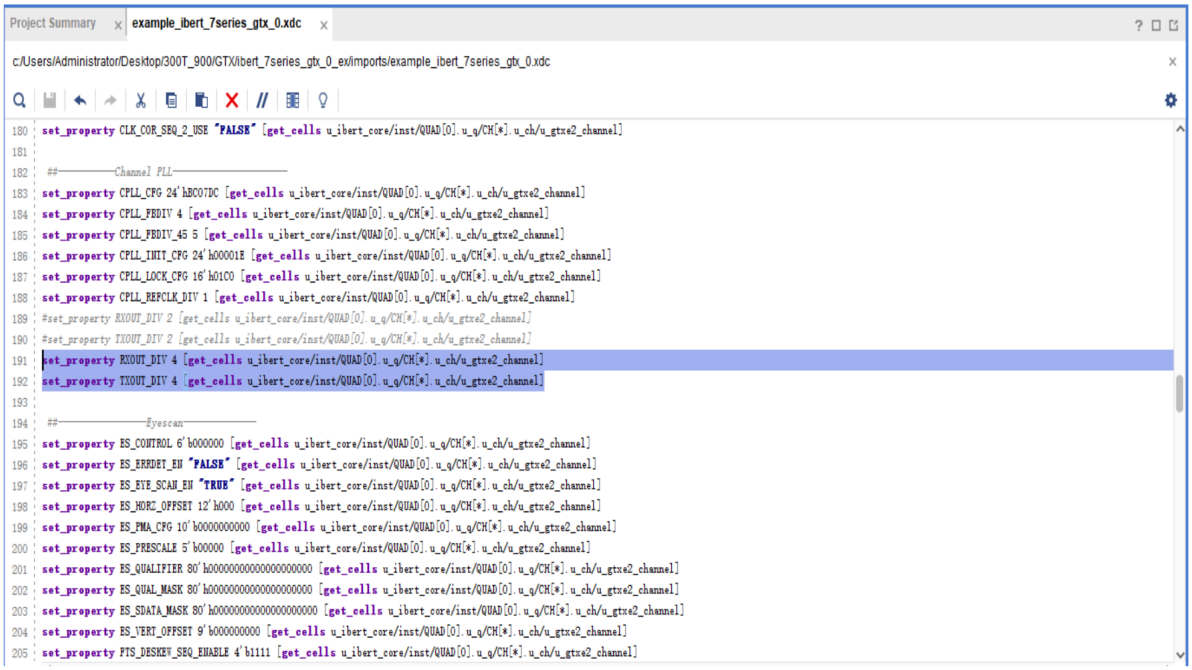


Figure 39. Change TX/RX division coefficient

Generate the bit file after the modifications above to resolve the QPLL incompatibility.

(2) XAUI IP

XAUI IP uses QPLL mode by default. The following describes how to make XAUI IP compatible.

Step 1: Set the IP data rate. At a XAUI IP data rate of 10Gb/s, each lane has a line rate of 3.125Gb/s; at 20Gb/s, each lane has a line rate of 6.25Gb/s. The example below describes the modification for 10Gb/s.

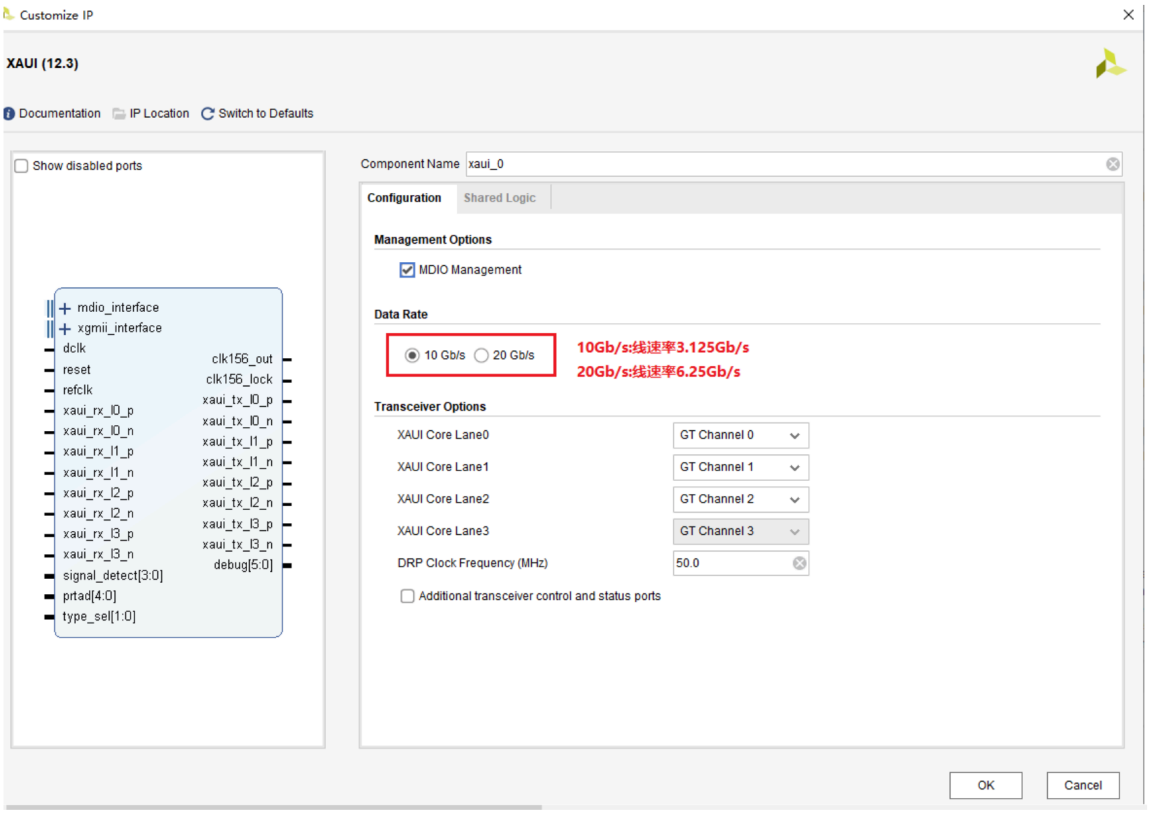


Figure 40. XAUI IP settings 1

Red annotation: 10Gb/s data rate: 3.125Gb/s line rate; 20Gb/s data rate: 6.25Gb/s line rate.

Step 2: Configure the Shared Logic screen as shown below, so that the GTX COMMON primitive is included in the IP.

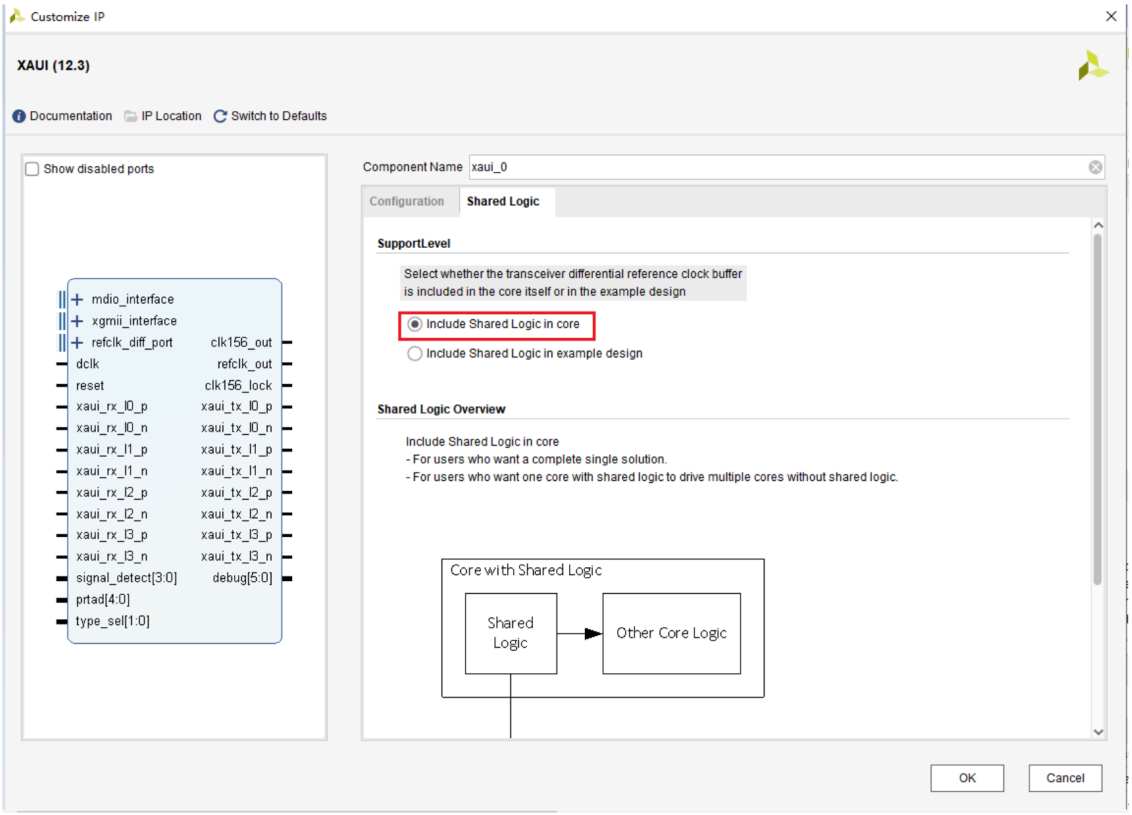


Figure 41. XAUI IP settings 2

Step 3: After setting up the IP, click OK. Set the IP synthesis mode to Global so that the underlying IP files can be modified, as shown below.

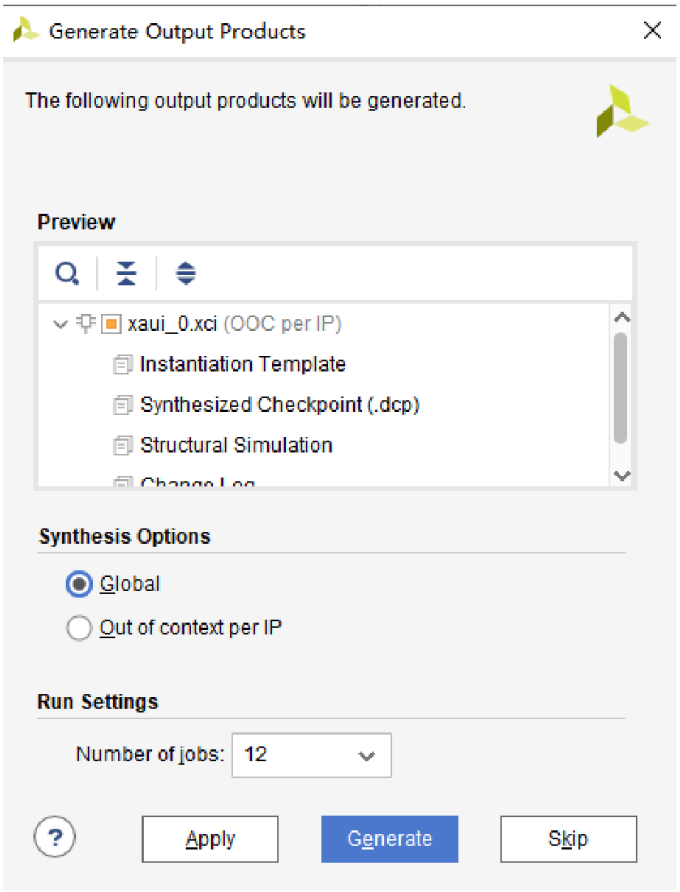


Figure 42. Set XAUI IP synthesis mode

Step 4: The solution is to set coefficient D to 4 (10Gb/s) or 2 (20Gb/s), and set coefficient N to 80. Locate the source files to be modified in the project path as shown below.

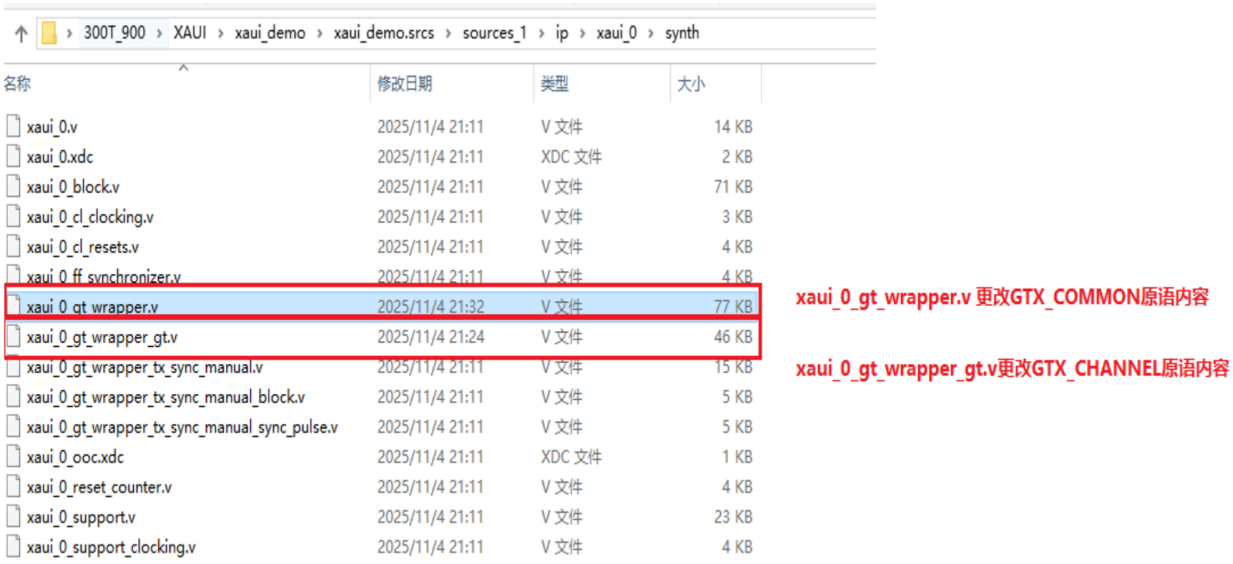


Figure 43. XAUI IP source file path

Red annotations: xaui_0_gt_wrapper.v — modify the GTX_COMMON primitive; xaui_0_gt_wrapper_gt.v — modify the GTX_CHANNEL primitive.

Modify the files as shown below. In the GTX_CHANNEL primitive, set RXOUT_DIV and TXOUT_DIV to 4 (or 2 when the 20Gb/s data rate is selected).

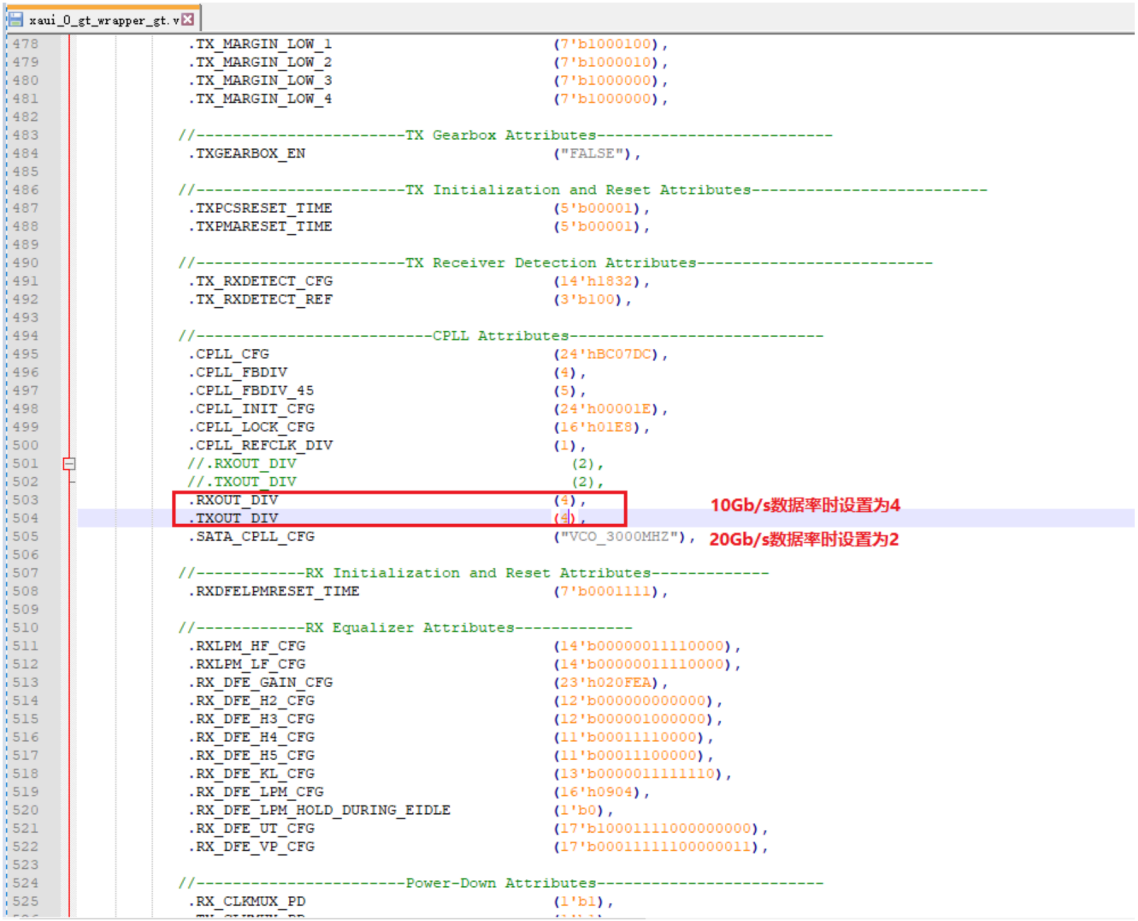
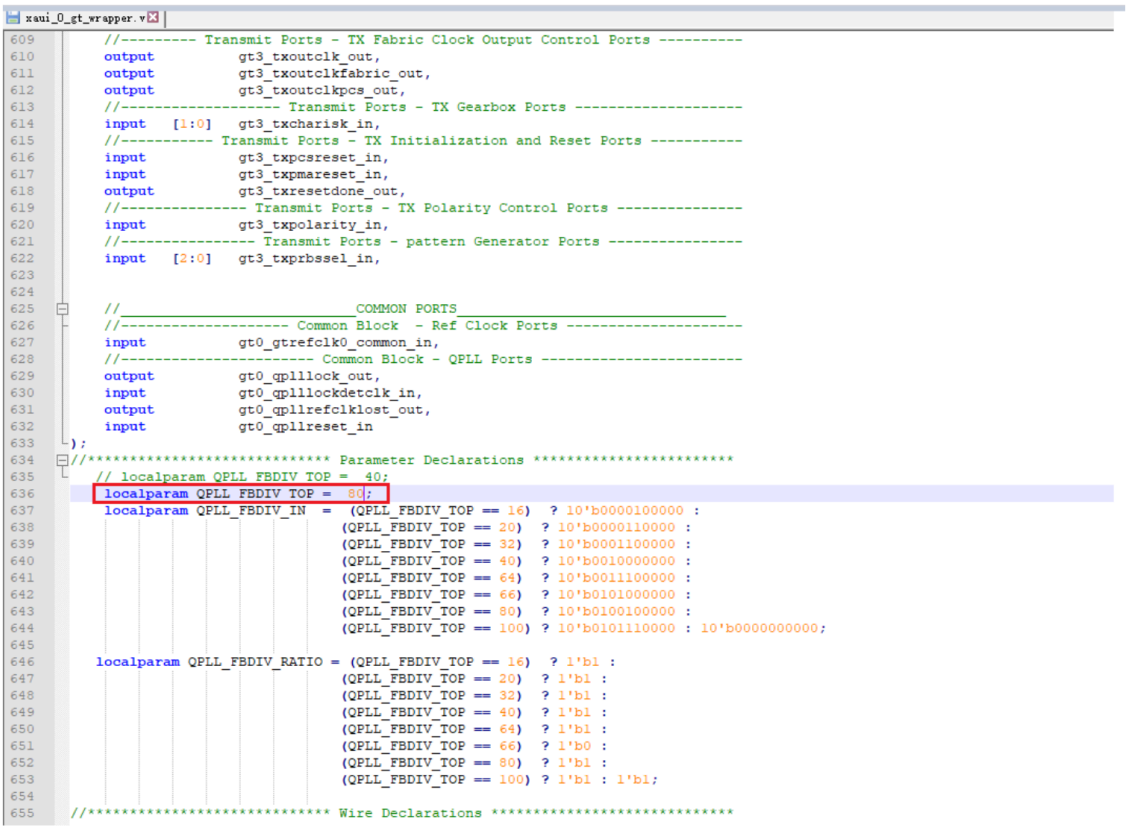


Figure 44. Change coefficient D in XAUI IP source file

Red annotations: Set to 4 for a 10Gb/s data rate; set to 2 for a 20Gb/s data rate.

Modify the GTX_COMMON primitive configuration as shown below.



```
xaui_0_gt_wrapper.v
609     //--------- Transmit Ports - TX Fabric Clock Output Control Ports ----------
610     output          gt3_txoutclk_out,
611     output          gt3_txoutclkfabric_out,
612     output          gt3_txoutclkpcs_out,
613     //------------------- Transmit Ports - TX Gearbox Ports --------------------
614     input   [1:0]   gt3_txcharisk_in,
615     //----------- Transmit Ports - TX Initialization and Reset Ports -----------
616     input           gt3_txpcsreset_in,
617     input           gt3_txpmareset_in,
618     output          gt3_txresetdone_out,
619     //---------------- Transmit Ports - TX Polarity Control Ports ----------------
620     input           gt3_txpolarity_in,
621     //----------------- Transmit Ports - pattern Generator Ports -----------------
622     input   [2:0]   gt3_txprbssel_in,
623
624
625     //____________________________COMMON PORTS_____________________________________
626     //-------------------- Common Block  - Ref Clock Ports ---------------------
627     input           gt0_gtrefclk0_common_in,
628     //----------------------- Common Block - QPLL Ports -------------------------
629     output          gt0_qplllock_out,
630     input           gt0_qplllockdetclk_in,
631     output          gt0_qpllrefclklost_out,
632     input           gt0_qpllreset_in
633 );
634 //***************************** Parameter Declarations ************************
635     // localparam QPLL_FBDIV_TOP =  40;
636     localparam QPLL_FBDIV_TOP =  80;
637     localparam QPLL_FBDIV_IN  =  (QPLL_FBDIV_TOP == 16)  ? 10'b0000100000 :
638                                  (QPLL_FBDIV_TOP == 20)  ? 10'b0000110000 :
639                                  (QPLL_FBDIV_TOP == 32)  ? 10'b0001100000 :
640                                  (QPLL_FBDIV_TOP == 40)  ? 10'b0001000000 :
641                                  (QPLL_FBDIV_TOP == 64)  ? 10'b0011100000 :
642                                  (QPLL_FBDIV_TOP == 66)  ? 10'b0101000000 :
643                                  (QPLL_FBDIV_TOP == 80)  ? 10'b0100100000 :
644                                  (QPLL_FBDIV_TOP == 100) ? 10'b0101110000 : 10'b0000000000;
645
646     localparam QPLL_FBDIV_RATIO = (QPLL_FBDIV_TOP == 16)  ? 1'b1 :
647                                   (QPLL_FBDIV_TOP == 20)  ? 1'b1 :
648                                   (QPLL_FBDIV_TOP == 32)  ? 1'b1 :
649                                   (QPLL_FBDIV_TOP == 40)  ? 1'b1 :
650                                   (QPLL_FBDIV_TOP == 64)  ? 1'b1 :
651                                   (QPLL_FBDIV_TOP == 66)  ? 1'b0 :
652                                   (QPLL_FBDIV_TOP == 80)  ? 1'b1 :
653                                   (QPLL_FBDIV_TOP == 100) ? 1'b1 : 1'b1;
654
655 //***************************** Wire Declarations *****************************
```

Figure 45. Change coefficient N in XAUI IP source file

Note: For both the 10Gb/s and 20Gb/s data-rate modes, the GTX_COMMON primitive must be modified as shown above.

Generate the bit file after the above modifications to resolve the XAUI IP incompatibility.

(3) RXAUI IP

RXAUI IP uses QPLL mode by default. The following describes how to make XAUI IP compatible (the procedure is the same as for XAUI).

Step 1: Configure the IP as shown below.

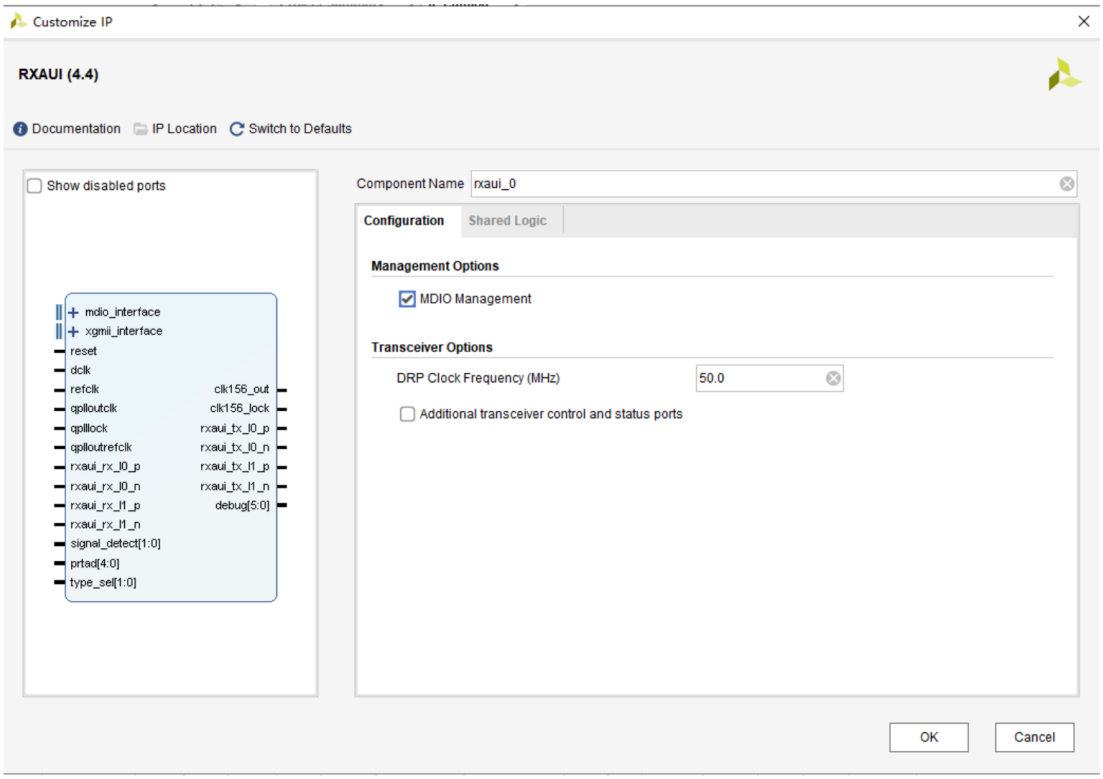


Figure 46. RXAUI IP settings 1

Step 2: Configure the Shared Logic screen as shown in Figure 47 below, so that the GTX COMMON primitive is included in the IP.

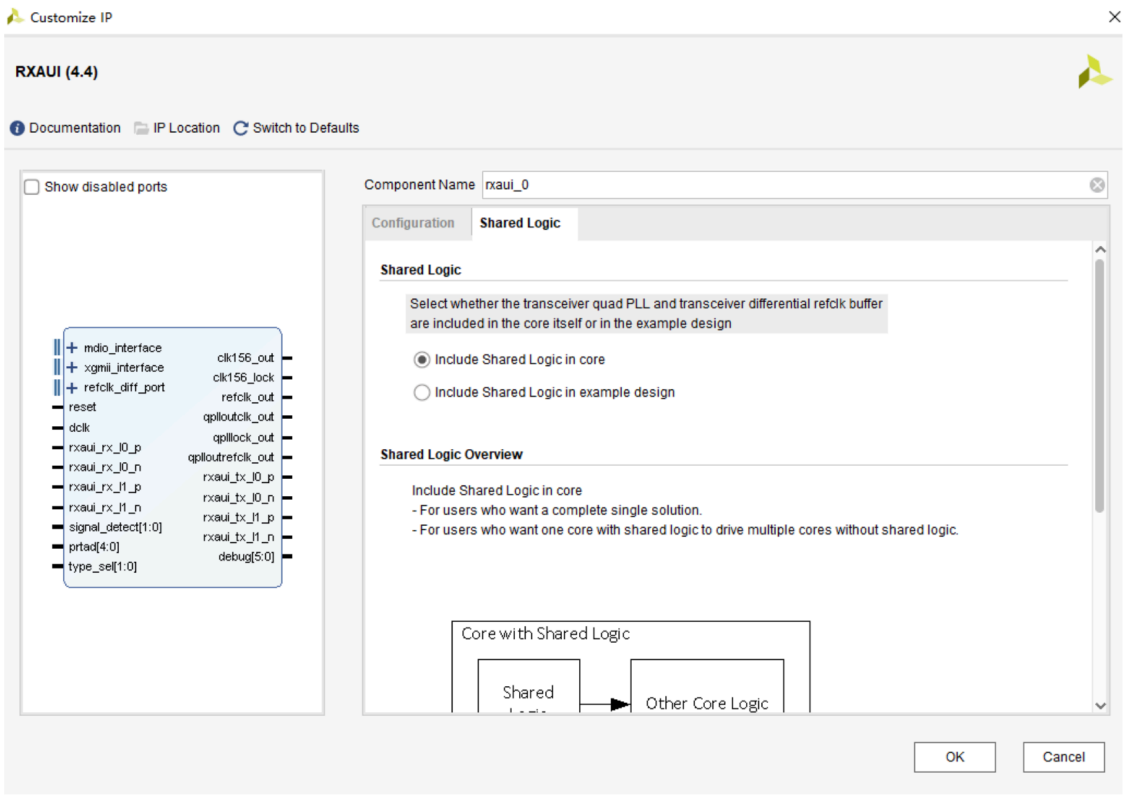


Figure 47. RXAUI IP settings 2

Step 3: Set the IP synthesis mode to Global so that the underlying IP files can be modified, as shown below.

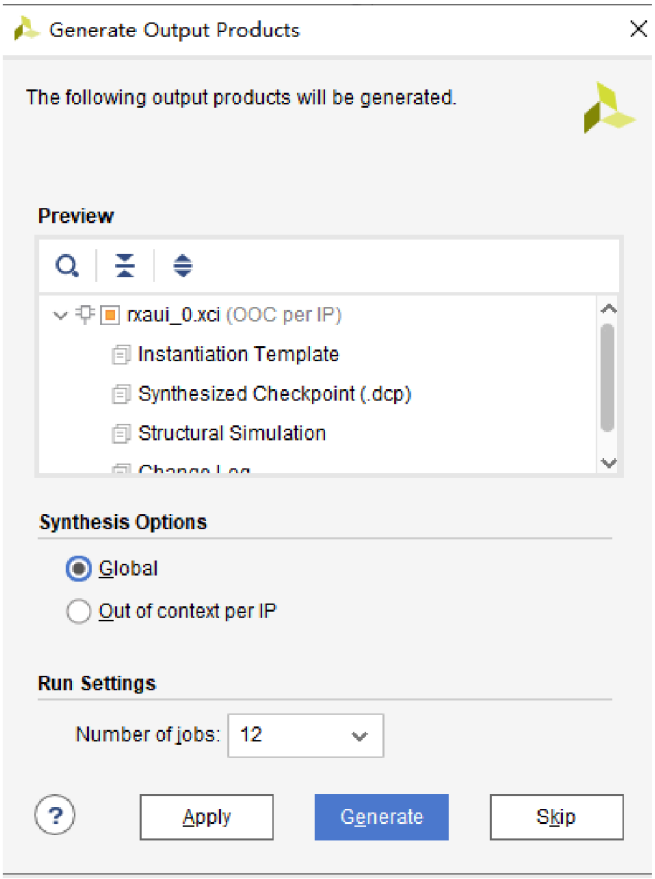


Figure 48. Set XAUI IP synthesis mode

Step 4: Modify the IP source files. The solution is to set coefficient D to 2 and coefficient N to 80. Locate the source files to be modified in the project path as shown below.

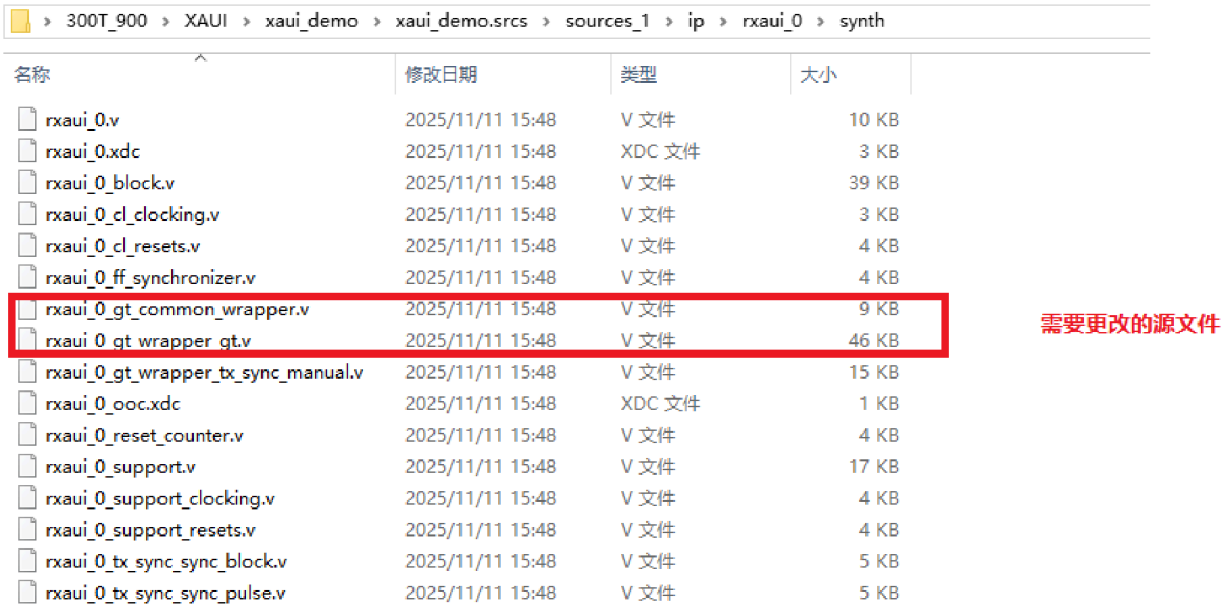
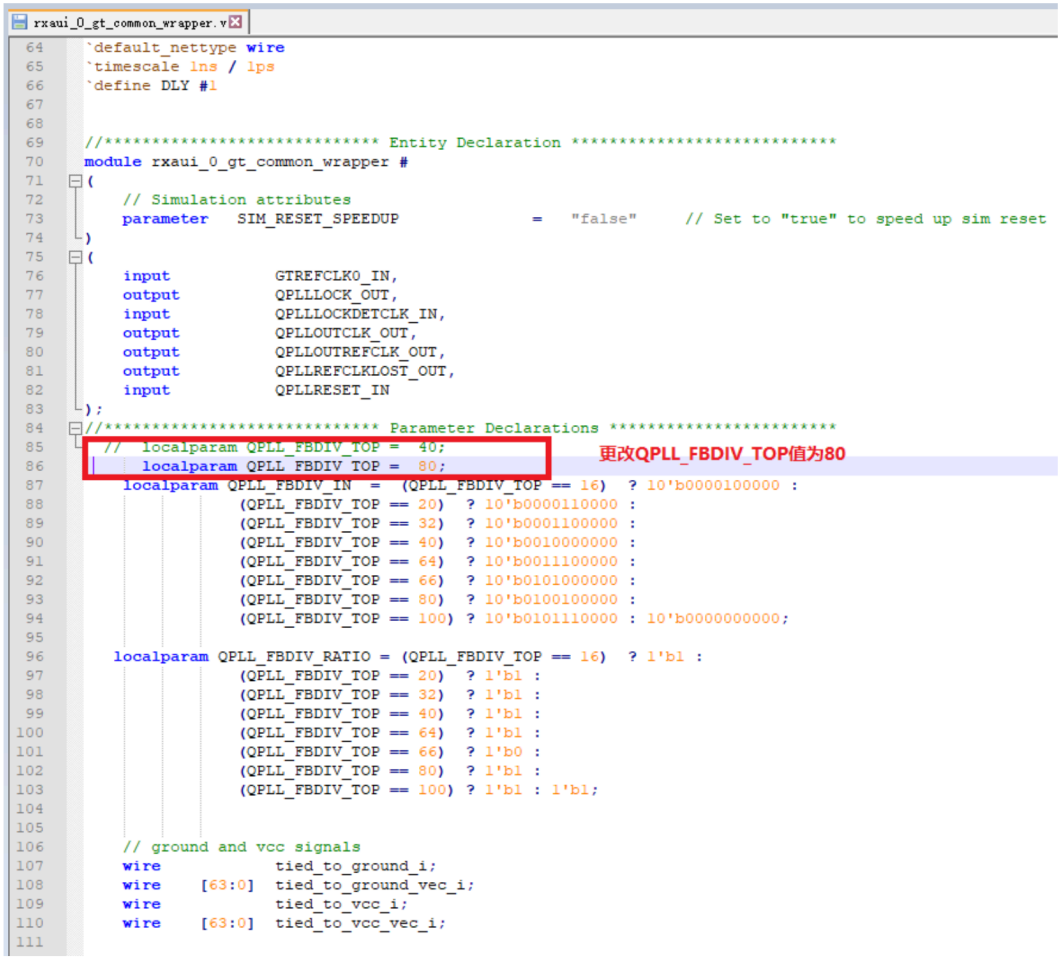


Figure 49. Path of source files to be modified

Red annotation: Source files requiring modification — rxaui_0_gt_common_wrapper.v and rxaui_0_gt_wrapper_gt.v.

Step 5: Open rxaui_gt_common_wrapper.v and modify the contents as shown below.




```
`default_nettype wire
`timescale 1ns / 1ps
`define DLY #1


//***************************** Entity Declaration ****************************
module rxaui_0_gt_common_wrapper #
(
    // Simulation attributes
    parameter   SIM_RESET_SPEEDUP             =   "false"     // Set to "true" to speed up sim reset
)
(
    input           GTREFCLK0_IN,
    output          QPLLLOCK_OUT,
    input           QPLLLOCKDETCLK_IN,
    output          QPLLOUTCLK_OUT,
    output          QPLLOUTREFCLK_OUT,
    output          QPLLREFCLKLOST_OUT,
    input           QPLLRESET_IN
);
//***************************** Parameter Declarations ************************
  //  localparam QPLL_FBDIV_TOP =  40;
    localparam QPLL_FBDIV_TOP =  80;
    localparam QPLL_FBDIV_IN  =  (QPLL_FBDIV_TOP == 16)  ? 10'b0000100000 :
                 (QPLL_FBDIV_TOP == 20)  ? 10'b0000110000 :
                 (QPLL_FBDIV_TOP == 32)  ? 10'b0001100000 :
                 (QPLL_FBDIV_TOP == 40)  ? 10'b0010000000 :
                 (QPLL_FBDIV_TOP == 64)  ? 10'b0011100000 :
                 (QPLL_FBDIV_TOP == 66)  ? 10'b0101000000 :
                 (QPLL_FBDIV_TOP == 80)  ? 10'b0100100000 :
                 (QPLL_FBDIV_TOP == 100) ? 10'b0101110000 : 10'b0000000000;

  localparam QPLL_FBDIV_RATIO = (QPLL_FBDIV_TOP == 16)  ? 1'b1 :
                 (QPLL_FBDIV_TOP == 20)  ? 1'b1 :
                 (QPLL_FBDIV_TOP == 32)  ? 1'b1 :
                 (QPLL_FBDIV_TOP == 40)  ? 1'b1 :
                 (QPLL_FBDIV_TOP == 64)  ? 1'b1 :
                 (QPLL_FBDIV_TOP == 66)  ? 1'b0 :
                 (QPLL_FBDIV_TOP == 80)  ? 1'b1 :
                 (QPLL_FBDIV_TOP == 100) ? 1'b1 : 1'b1;


    // ground and vcc signals
    wire            tied_to_ground_i;
    wire    [63:0]  tied_to_ground_vec_i;
    wire            tied_to_vcc_i;
    wire    [63:0]  tied_to_vcc_vec_i;
```

Figure 50. GTX_COMMON primitive modifications

Red annotation: Change QPLL_FBDIV_TOP to 80.

Open rxaui_gt_wrapper.v and modify the contents as shown below.

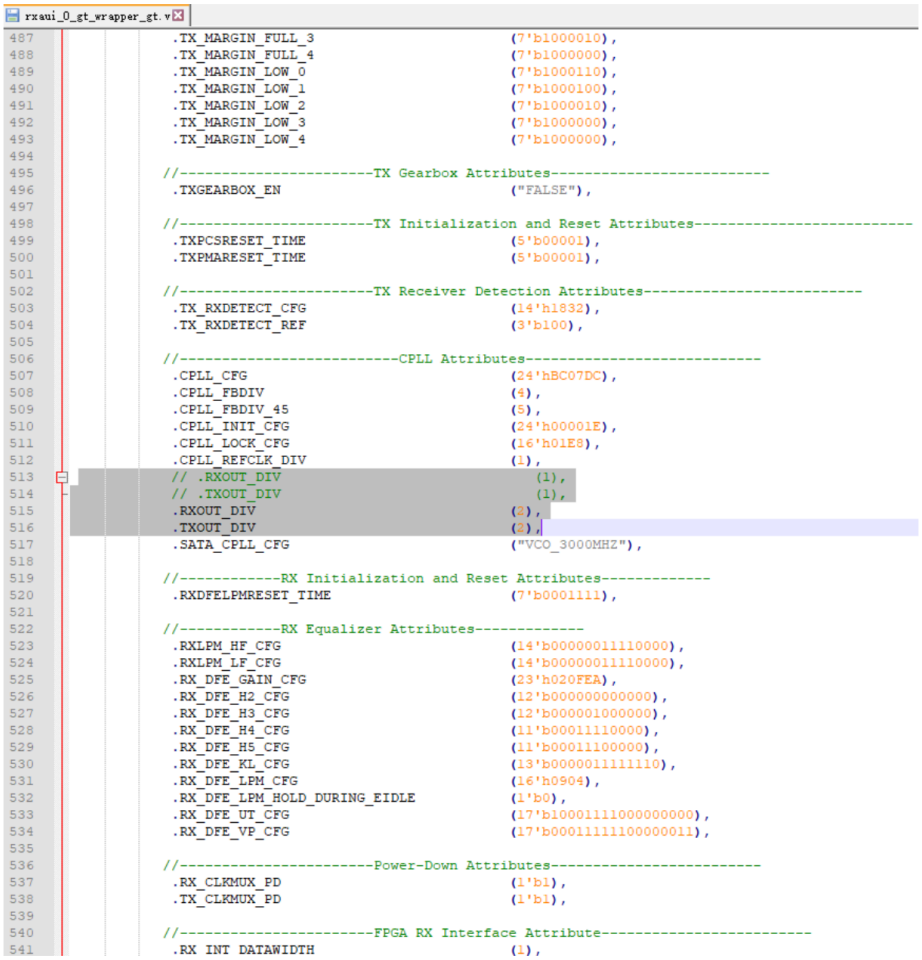


Figure 51. GTX_CHANNEL primitive modifications

Generate the bit file after the above modifications to resolve the RXAUI IP incompatibility.

8.10 VCCO supply recommendations for an unused HRIO BANK

When an entire HRIO BANK is unused, its VCCO can be connected to 1.8V, 2.5V or 3.3V, or left floating. If grounded, connect a series resistor greater than 4K to ground; otherwise direct grounding may increase the VCCAUX static current. When an HPIO BANK is unused, its VCCO can be grounded directly.

9. Usage precautions

Observe the following precautions when operating the device:

a) Strictly observe the recommended operating conditions. Operation beyond the absolute maximum ratings may cause permanent damage to the product;

b) Power-up method: The PS and PL supplies are completely independent, and each side has its own recommended power-up sequence. The PS can operate with the PL power supply turned off. If the PL must be in a powered-down mode during use, it is recommended to power up the PS before the PL. If the PL does not need to be powered down, some supply rails of the two sides may share the same power supply;

c) Handle the device on an antistatic workbench;

d) Ground test equipment and instruments;

e) Do not touch the device leads;

f) Store devices in containers made of conductive materials;

g) Avoid plastics, rubber and silk fabrics that can generate static electricity in the MOS area.

10. Ordering information

Table 63. Product ordering information

No.	Product model	Package	Package material	Quality grade	Solder ball material	Weight (g)	Detailed spec.
1	EKT7Z045FFG900M3	PBGA900	Plastic	N1 grade	Sn96.5/Ag3.0/Cu0.5	11.85±1.5 (with solder balls)	
2	EKT7Z045FFG900E	PBGA900	Plastic	Military temperature grade	Sn96.5/Ag3.0/Cu0.5	11.85±1.5 (with solder balls)	
3	EKT7Z045FFG900I	PBGA900	Plastic	Industrial temperature grade	Sn96.5/Ag3.0/Cu0.5	11.85±1.5 (with solder balls)	

Note 1:

a) N/N1 grade devices meet the screening requirements for N/N1 grade in GJB 7400A, General Specification for Semiconductor Integrated Circuits under Qualified Manufacturer Certification;

b) Industrial temperature-grade devices meet the screening requirements of Q, General Specification for Industrial Temperature-Grade Products (source manufacturer standard). Their operating ambient temperature range or junction temperature is −40°C to +85°C.

c) Military temperature-grade devices meet the screening requirements of Q, General Specification for Military Temperature-Grade Products (source manufacturer standard). Their operating ambient temperature range or junction temperature is −55°C to +125°C.

Note 2: Product ordering information covers existing products or devices planned for development. Other package types can be developed according to user requirements.